SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS (DECS)

COURSE STRUCTURE

I Year – I Semester

S.No.	Course code	Subject	L	T	P	CP
1.	16EC3801	Digital System Design	4	-	-	4
2.	16EC3802	Advanced Digital Signal Processing	4	-	-	4
3.	16EC3803	Digital Communication Techniques	4	-	-	4
4.	16EC3804	Adaptive Signal Processing	4	-	-	4
5.	16EC5502	Embedded System Concepts	4	-	-	4
ELECTIVE I						
6.	16EC5503	Advanced Computer Architectures	4	-	-	4
7.	16EC3805	DSP Processors & Architectures			-	
8.	16EC5709	Low Power VLSI Design			-	
LABORATORY						
9.	16EC3806	Communications & Signal Processing Lab	-	-	4	2
Contact periods / week			24	-	4	**26**
			Total/Week		**28**	

I Year – II Semester

S.No.	Course code	Subject	L	T	P	CP
1.	16EC3807	Micro Computer System Design	4	-	-	4
2.	16EC3808	Image & Video Processing	4	-	-	4
3.	16EC3809	Wireless Communications	4	-	-	4
4.	16EC3810	Coding Theory & Techniques	4	-	-	4
5.	16EC3811	Detection & Estimation of Signals	4	-	-	4
ELECTIVE II						
6.	16EC3812	Hi-Speed Networks	4	-	-	4
7.	16EC3813	Optical Networks				
8.	16EC3814	Compression Techniques				
LABORATORY						
9.	16EC3815	Digital System Design Lab	-	-	4	2
Contact Periods / Week			24	-	4	**26**
			Total/Week		**28**	

II YEAR (III & IV Semesters)

S.No	Subject Code	Subject	Credits
1	16EC3816	Seminar	2
2	16EC3817	Project work	16

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3801) DIGITAL SYSTEM DESIGN

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, Design of sequential circuits using ROMs, PLAs, CPLD and FPGAs

UNIT II

FAULT MODELING: Fault classes and models – Stuck at faults, Bridging faults, Transition and Intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods– Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT III

TEST PATTERN GENERATION: D – Algorithm, PODEM, Random testing, Transition count testing, Signature Analysis and Testing for bridging faults.

UNIT IV

PROGRAMMING LOGIC ARRAYS: Introduction, Design using PLA's, PLA minimization and PLA folding.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and Fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT V

PLA TESTING: Fault models, Test generation and Testable PLA design.

ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, Flow table, State reduction, Minimal closed covers, Races, Cycles and Hazards.

TEXTBOOKS:

1. *Switching & finite Automata Theory,* Z. Kohavi , (TMH)
2. *Logic Design Theory,* N. N. Biswas,– (PHI)
3. *Digital Logic Design Principles,* Nolman Balabanian, Bradley Calson Wily Student Edition 2004.

REFERENCES:

1. *Digital System Testing and Testable Design,* M. Abramovici, M. A. Breues, A. D. Friedman, Jaico Publications.
2. *Fundamentals of Logic Design,* Charles H. Roth Jr.
3. *Computer Aided Logic Design,* Frederick. J. Hill & Peterson, Wiley 4th Edition.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3802) ADVANCED DIGITAL SIGNAL PROCESSING

M.Tech I Year -I SEM (DECS) **L T C**
4 - 4

UNIT I

OVERVIEW : Discrete-Time Signals, Sequences and sequence Representation, Discrete-Time Systems, Time-Domain Characterization and Classification of LTI Discrete-Time Systems. The Continuous-Time Fourier Transform, The discrete-Time Fourier Transform, energy Density Spectrum of a Discrete-Time Sequence, Band-Limited Discrete-Time signals, The Frequency Response of LTI Discrete-Time System.

LTI SYSTEMS: Types of Linear-Phase transfer functions, Simple Digital Filters, Complementary Transfer Function, Inverse Systems, System Identification, Digital Two-Pairs, Algebraic Stability Test.

UNIT II

DIGITAL FILTER SRTUCTURE AND DESIGN: All Pass Filters, Tunable IIR Digital Filter, IIR Tapped Cascade Lattice Structures, FIR Cascaded Lattice Structures, Parallel All Pass Realization of IIR Transfer Functions, State Space Structures, Polyphase Structures, Digital Sine-Cosine Generator, Computational Complexity of Digital Filter Structures, Design of IIR Filter using pade approximation, Least Square Design Methods, Design of Computationally Efficient FIR Filters.

UNIT III

FFT ALGORITHEMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT IV

POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.

PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT V

ANALYSIS OF FINITE WORDLENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS: Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality-Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Non stationary Signals, Musial Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete-Time Analytic Signal Generation.

TEXTBOOKS:

1. *Digital Signal Processing*, Sanjit K Mitra, Tata MCgraw Hill Publications.
2. *Digital Signal Processing Principles*, Algorithms, Applications by J G Proakis, D G Manolokis, PHI.

REFERENCES:

1. *Discrete-Time Signal Processing*, A V Oppenhiem, R W Schafer, Pearson Education.
2. *DSP- A Practical Approach*, Emmanuel C Ifeacher Barrie. W. Jervis, Pearson Education.
3. *Modern spectral Estimation techniques*, S. M .Kay, PHI, 1997

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3803) DIGITAL COMMUNICATION TECHNIQUES

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

REVIEW OF RANDOM VARIABLES AND PROCESSES: Random variable – Moment generating function – Markov‟s inequality – Chebyshev‟s inequality – Central limit theorem– Chi-square, Rayleigh, and Ricean distributions – Correlation – Covariance matrix Stationary processes – Wide sense stationary processes – Ergodic process – Cross correlation – Autocorrelation functions – Gaussian process.

CHARACTERIZATION OF COMMUNICATION SIGNALS AND SYSTEMS: Signal space representations- Vector Space Concepts, Signal Space Concepts, Orthogonal Expansion of Signals. Representation of Digitally Modulated Signals-Memory less Modulation Methods.

UNIT II

COMMUNICATION OVER ADDITIVE GAUSSIAN NOISE CHANNELS : Optimum receiver for signals corrupted by additive white Gaussian noise (AWGN)- Cross correlation demodulation, matched filter demodulator and error probabilities.

Optimum receiver for signals with random phase in AWGN channels, Optimum receiver for binary signals, Optimum receiver for M-array orthogonal signals, Probability of error for envelope detection of Mary orthogonal signals. Optimum waveform receiver for colored Gaussian noise channels, Karhunen-Loeve expansion approach, and whitening.

UNIT III

FADING CHANNELS: Characterization of fading multipath channels, Statistical Models for fading channels, Time varying Channel impulse response, narrow and wide band fading models, channel correlation functions, Key multipath parameters, Rayleigh and Ricean fading channels, Simulation methodology of fading channels.

UNIT IV

DIGITAL COMMUNICATION OVER FADING CHANNELS: Optimum coherent and non-coherent receiver in random amplitude, random phase channels- Performance of Rayleigh and Ricean channels, Performance of digital Modulation schemes such as BPSK, QPSK,FSK, DPSK, MSK etc. over wireless channels.

UNIT V

COMMUNICATION OVER BAND LIMITED CHANNELS: Communication over band Limited Channels- Optimum pulse shaping- Nyquist criterion for zero ISI, partial response signaling- Equalization Techniques, Zero forcing linear Equalization- Decision feedback equalization.

ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (OFDM): Carrier Synchronization, Timing synchronization, Multichannel and Multicarrier Systems.

TEXT BOOKS:

1. *Digital Communications*, J. Proakis, McGraw Hill, 2000
2. *Principles of Digital Communications and Codin,* J. Viterbi and J. K. Omura, McGraw Hill,1979
3. *Spread Spectrum Communications,* Marvin K. Simon, Jim K Omura, Robert A. Scholtz, Barry K.Levit,1995.
4. *CDMA Principles of Spread Spectrum Communications,* Andrew J Viterbi, Addison Wesley,1995.

REFERENCES:

1. *Multi-carrier Digital Communications*: *Theory and Applications of OFDM*, Ahmad R S Bahai, Burton R Saltzberg Mustafa Ergen, Springer Publications.
2. *Digital Communication,* J.S.Chitode, Technical Publications.
3. *Digital Communication,* Edward. A. Lee and David. G. Messerschmitt, 2/e, Allied Publishers.
4. *Digital Communication Techniques* J Marvin.K.Simon, Sami. M. Hinedi and William. C. Lindsey, PHI.
5. *An introduction to Probability Theory and its applications,* William Feller, Vol 11, Wiley2000.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY PUTTUR
(AUTONOMOUS)
(16EC3804) ADAPTIVE SIGNAL PROCESSING

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

EIGEN ANALYSIS: Eigen Value Problem, Properties of eigen values and eigen vectors, Eigen Filters, eigen Value computations.

INTRODUCTION TO ADAPTIVE SYSTEMS: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner - Description, Weight Vectors, Desired Response Performance function, Gradient & Mean Square Error.

UNIT II

DEVELOPMENT OF ADAPTIVE FILTER THEORY & SEARCHING THE PERFORMANCE SURFACE: Introduction to Filtering, Smoothing and Prediction, Linear Optimum Filtering, Problem statement, Principle of Orthogonality - Minimum Mean Square Error, Wiener- Hopf equations, Error Performance - Minimum Mean Square Error.

SEARCHING THE PERFORMANCE SURFACE – Methods & Ideas of Gradient Search methods, Gradient Searching Algorithm & its Solution, Stability & Rate of convergence - Learning Curves.

UNIT III

STEEPEST DESCENT ALGORITHMS: Gradient Search by Newton's Method, Method of Steepest Descent, Comparison of Learning Curves.

LMS ALGORITHM & APPLICATIONS: Overview - LMS Adaptation algorithms, Stability & Performance analysis of LMS Algorithms - LMS Gradient & Stochastic algorithms, Convergence of LMS algorithm.

Applications: Noise cancellation, Cancellation of Echoes in long distance telephone circuits, Adaptive Beam forming.

UNIT-IV

RLS ALGORITHM: Matrix Inversion lemma, Exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, convergence analysis of RLS Algorithm, Application of RLS algorithm on Adaptive Equalization

UNIT V

KALMAN FILTERING: Introduction, Recursive Mean Square Estimation Random variables, Statement of Kalman filtering problem, Filtering, Initial conditions, Variants of Kalman filtering, Extend Kalman filtering.

NON LINEAR ADAPTIVE FILTERING: Theoretical and Practical considerations of Blind Deconvolution, Buss Gang Algorithm for blind Equalization of real baseband Channels.

TEXT BOOKS:

1. *Adaptive Signal Processing*, Bernard Widrow, Samuel D.Strearns, 2005, PE.
2. *Adaptive Filter Theory*, Simon Haykin, 4 ed., 2002, PE Asia.

REFERENCES:

1. *Optimum signal processing: An introduction*, Sophocles.J.Orfamadis, 2 ed., 1988, McGraw-Hill, New York
2. *Adaptive signal processing-Theory and Applications*, S.Thomas Alexander, 1986, Springer –Verlag.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5502) EMBEDDED SYSTEM CONCEPTS

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded Software in a system, embedded system on chip (SOC), design process, classification of embedded systems

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication Interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT II

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT III

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

UNIT IV

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

UNIT V

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1.*Computers as a component: principles of embedded computing system design*-Wayne wolf
2.*An embedded software premier*: David E. Simon
3.*Embedded / real time systems*-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. *Embedded real time systems programming*-sri ram V Iyer, pankaj gupta, TMH, 2004
2 *Embedded system design - A unified hardware/software introduction* - frank vahid, tony D.Givargis, John Willey, 2002

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5503) ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE I)

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Elements of modern computers, Technology trends, cost-measuring and reporting performance quantitative principles of computer design.

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set-the role of compiler.

UNIT II

INSTRUCTION LEVEL PARALLELISM (ILP): overcoming data hazards, reducing branch costs, high performance instruction delivery, and hardware based speculation, limitation of ILP.

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions.

UNIT III

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi-threading.

UNIT IV

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT V

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster.

TEXTBOOKS:

1. *Computer Architecture A quantitative approach*, 3rd edition (An Imprint of Elsevier)John. Hennessy & David A. Patterson Morgan Kufmann,

REFERENCES:

1. *Computer Architecture and parallel Processing*, International Edition McGraw-Hill. Kai Hwang and A. Briggs,
2. *Advanced Computer Architectures*, Pearson Dezso Sima, Terence Fountain, Peter Kacsuk,

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3805) DSP PROCESSORS & ARCHITECTURES
(ELECTIVE I)

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT III PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. *Digital Signal Processing*, Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. *DSP Processor Fundamentals, Architectures & Features*, Lapsley et al. S.Chand & Co, 2000.

REFERENCES:

1. *Digital Signal Processors, Architecture, Programming and Applications*, B.Venkata Ramani and M. Bhaskar, TMH, 2004.
2. *Digital Signal Processing*, Jonatham Stein, John Wiley, 2005.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5709) LOW POWER VLSI DESIGN
(ELECTIVE I)

M.Tech I Year -I SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/Bi-CMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT II

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT III

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT IV

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT V

SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1. *CMOS/BiCMOS ULSI low voltage, low power,* Yeo Rofail/ Gohl(3 Authors), Pearson Education Asia 1st Indian reprint,2002.
2. *Practical Low Power Digital VLSI Design,* Gary K. Yeap, KAP, 2002.

REFERENCES:

1. *Basic VLSI Design,* Douglas A.Pucknell & Kamran Eshraghian, 3rd edition PHI.
2. *Digital Integrated circuits,* J.Rabaey,PH,1996
3. *CMOS Digital ICs,* Sung-mo Kang and yusuf leblebici,3rd edition TMH 2003.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3806) COMMUNICATIONS & SIGNAL PROCESSING LAB

M.Tech I Year -I SEM (DECS) **L P C**
0 4 2

1. Simulation Rayleigh Fading Channel Using Either Clarke‟s Model or Jake‟s Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
2. Generation of Maximal Sequences and Gold Sequences.
3. Design and Simulation FIR Filter Using any Windowing Technique.
4. Design of IIR Filters from Analog Filters.
5. Performance Evaluation of QPSK System over Gaussian AWGN Channel.
6. Performance Evaluation of QPSK System over Rayleigh Fading Channel.
7. Equalization of Multipath Channel using LMS or RLS Algorithms.
8. Performance Evaluation of RAKE Receiver over Slow Fading Channel.

NOTE: Use Mat lab

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3807) MICRO COMPUTER SYSTEM DESIGN

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures.

THE 80286 MICRO PROCESSORS: Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNIT II

THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

THE PENTIUM AND PENTIUM PRO PROCESSORS: The Memory System, Input/output system, Branch Prediction Logic, Cache Structure, Pentium Registers, Serial Pentium pro features.

UNIT III

THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

INTRODUCTION TO MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Memory Management, Virtual Memory Concept of 80286 and other advanced Processors.

UNIT IV

ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

UNIT V

8096-MICROCONTROLLER: Introduction, Compare and contrast with 8051 microcontroller, Architecture and features, RAM structure, Register organization, Interrupts, Ports, Addressing modes and Instruction Set (brief treatment).

TEXTBOOKS:

1. *The Intel Microprocessors*, Barry, B. Brey, 8th Edition Pearson Education, 2009.
2. *Advanced Microprocessor and Peripherals,* A.K. Ray and K.M. Bhurchandi, TMH.
3. *Microprocessors and microcontrollers: Architecture, programming and System design 8085, 8086, 8051, 8096,* Kant, Krishna, 2nd Edition.

REFERENCES:

1. *Micro Computer Systems: The 8086/8088 Family Architecture, Programming and Design* YU-Chang, Glenn A. Gibson, 2nd Edition, Pearson Education, 2007.
2. *Microprocessors and Interfacing,* Douglas V. Hall, "" Special Indian Edition, 2006.
3. *Field Programmable Gate Array,* S.Brown, R.Francis, J.Rose, Z.Vransic, Kluwer Pubin, 1992

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3808) IMAGE & VIDEO PROCESSING

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

IMAGE REPRESENTATION: Gray scale and color Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WT, Haar transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Filters in spatial and frequency domains, histogram-based processing, and homomorphic filtering. Edge detection, non-parametric and model based approaches, LOG filters, localization problem.

UNIT III

IMAGE RESTORATION: Degradation Models, PSF, circulant and block–circulant matrices, Deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods ,Morphological operations.

IMAGE SEGMENTATION: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Hough transform, Region growing.

UNIT IV

IMAGE COMPRESSION: Compression models, Information theoretic perspective, Fundamental coding theorem.

LOSSLESS COMPRESSION: Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT V

VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation, Motion compensation, Video Filtering, Video Compression, Video coding standards.

TEXT BOOKS:

1. *Digital Image Processing* R. C. Gonzalez, R. E. Woods, Pearson Education. 2nd edition, 2002
2. *Digital image processing*, W. K. Pratt, Prentice Hall, 1989
3. *Digital image processing*, A. Rosenfold and A. C. Kak, Vols. 1 and 2, Prentice Hall, 1986.

REFERENCES:

1. *Digital image restoration* H. C. Andrew and B. R. Hunt, Prentice Hall, 1977
2. *Machine Vision*, R. Jain, R.Kasturi and B.G.Schunck, McGraw-Hill International Edition, 1995.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3809) WIRELESS COMMUNICATIONS

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION TO WIRELESS COMMUNICATIONS SYSTEMS: Evolution, Examples of Wireless Communication systems, Comparison, Second Generation Cellular Networks, WLL, Bluetooth and Personal Area Networks.

UNIT II

MOBILE RADIO PROPAGATION: Large-Scale Path Loss, Introduction to Radio Wave Propagation, Free Space Propagation Model, Propagation Mechanisms, Reflection, Ground Reflection (Two-Ray) Model, Diffraction, Scattering. Small-Scale Fading and Multipath, Impulse Response Model of a Multipath Channel, Small- Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-Scale Fading, Rayleigh and Ricean Distributions, Statistical Models for Multipath Fading Channels, Theory of Multipath Shape Factors for Small-Scale Fading Wireless Channels.

UNIT III

DIVERSITY TECHNIQUES: Repetition coding and Time Diversity- Frequency and Space Diversity, Receive Diversity- Concept of diversity branches and signal paths- Combining methods- Selective diversity combining - Switched combining- maximal ratio combining- Equal gain combining- performance analysis for Rayleigh fading channels.

CELLULAR COMMUNICATION: Cellular Networks, Multiple Access: FDM/TDM/FDMA/TDMA, Spatial reuse, Co-channel interference Analysis, Hand over Analysis, Erlang Capacity Analysis, Spectral efficiency and Grade of Service- Improving capacity – Cell splitting and sectorization.

UNIT IV

SPREAD SPECTRUM AND CDMA: Motivation- Direct sequence spread spectrum- Frequency Hopping systems, Time Hopping., Anti-jamming- Pseudo Random (PN) sequence, Maximal length sequences, Gold sequences, Generation of PN sequences.

DIVERSITY IN DS-SS SYSTEMS: Rake Receiver- Performance analysis. Spread Spectrum Multiple Access, CDMA Systems- Interference Analysis for Broadcast and Multiple Access Channels, Capacity of cellular CDMA networks- Reverse link power control, Hard and Soft hand off strategies.

UNIT V

FADING CHANNEL CAPACITY: Capacity of Wireless Channels- Capacity of flat and frequency selective fading channels, Multiple Input Multiple output (MIMO) systems- Narrow band multiple antenna system model, Parallel Decomposition of MIMO Channels- Capacity of MIMO Channels.

CELLULAR WIRELESS COMMUNICATION STANDARDS: GSM specifications and Air Interface, specifications, IS 95 CDMA- 3G systems: UMTS & CDMA 2000 standards and specifications.

TEXT BOOKS:

1. *Wireless Communications,* Andrea Goldsmith, Cambridge University press.
2. *Modern Wireless Communications* Simon Haykin and Michael Moher, Person Education.
3. *Wireless Communication, principles & practice* T.S. Rappaport, PHI, 2001.

REFERENCES:

1. *Principles of Mobile Communications* G.L Stuber, 2ndedition, Kluwer Academic Publishers.
2. *Wireless digital communication* Kamilo Feher, PHI, 1995.
3. *Introduction to Spread Spectrum Communication* R.L Peterson, R.E. Ziemer and David E. Borth, Pearson Education.
4. *CDMA- Principles of Spread Spectrum,* A.J.Viterbi, Addison Wesley, 1995.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3810) CODING THEORY & TECHNIQUES

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

SOURCE CODING-I: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for Discrete less sources, Source coding theorem, fixed length and variable length coding, properties of prefix codes.

UNIT II

CODING TECHNIQUES: Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

LINEAR BLOCK CODES: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and correcting capability of Linear Block codes.

UNIT III

Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage Systems.

UNIT IV

CYCLIC CODES: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

CONVOLUTIONAL CODES: encoding of Convolutional codes, Structural properties of Convolutional codes, state diagram, Tree diagram, Trellis Diagram, maximum, Likelihood decoding of Convolutional codes.

UNIT V

Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.

BCH CODES: Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2m), Basic properties of Falois Fields, Computation using Falois Field GF (2m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

TEXT BOOKS:

1. *Error Control Coding – Fundamentals and Applications* SHU LIN and Daniel J. Costello, Jr.Prentice Hall Inc.
2. *Digital Communications-Fundamental and Application* Bernard sklar, Pearson Education, Asia.
3. *Error Control Coding Theory*, Man Young Rhee, McGraw Hill Publications.

REFERENCES:

1. *Digital Communications*, John G. Proakis, Mc. Graw Hill Publication.
2. *Digital and Analog Communication Systems* K. Sam Shanmugam, Wisley Publications.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3811) DETECTION & ESTIMATION OF SIGNALS

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

DETECTION THEORY: Binary decisions - Single observation- Maximum likelihood decision criterion, Neymann-Pearson criterion, Probability of error criterion, Bayes risk criterion, Min-max criterion, Robust detection, Receiver operating characteristics.

UNIT II

BINARY DECISIONS - MULTIPLE OBSERVATIONS: Vector observations, the general Gaussian Problem, Waveform Observation in Additive Gaussian Noise, The Integrating Optimum Receiver; Matched Filter Receiver.

UNIT III

ESTIMATION THEORY: Methods -Maximum likelihood estimation; Bayes cost method Bayes estimation criterion - Mean square error criterion; Uniform cost function; absolute value cost function; Linear minimum variance - Least squares method; Estimation in the presence of Gaussian noise - Linear observation; Non-linear estimation.

UNIT IV

PROPERTIES OF ESTIMATORS: Bias, Efficiency, Cramer-Rao bound Asymptotic properties, Sensitivity and error analysis.
STATE ESTIMATION: Prediction, Kalman filter.

UNIT V

SUFFICIENT STATISTICS AND STATISTICAL ESTIMATION OF PARAMETERS: Concept of sufficient statistics, Exponential families of Distributions, Exponential families and Maximum likelihood estimation, uniformly minimum variance unbiased estimation.

TEXT BOOKS:

1. *Decision and Estimation Theory*, James L. Melsa and David L. Cohn, McGraw Hill, 1978.
2. *Detection and Estimation*, Dimitri Kazakos, P. Papantoni Kazakos, Computer Science Press, 1990.
3. *Statistical Signal Processing: Vol.1: Estimation Theory, Vol. 2: Detection Theory,* Steven M. Kay, Prentice Hall Inc., 1998.

REFERENCES:

1. *Detection, Estimation and Modulation Theory, Part 1*,Harry L. Van Trees, John Wiley & Sons Inc. 1968.
2. *Lessons in Estimation Theory for Signal Processing, Communication and Control*, Jerry M. Mendel, Prentice Hall Inc., 1995.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3812) HI-SPEED NETWORKS
(ELECTIVE II)

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture.

UNIT II

ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT III

ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections.
QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT IV

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Routing algorithm & blocking phenomenon, Batcher-Banyan networks, crossbar switch, three stage class networks.
REARRANGEABLE NETWORKS: Re-arrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT V

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.
TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, Motivation, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue management: Passive & active, QOS in IP networks: differentiated and integrated services.

TEXT BOOKS:

1. *ISDN & B-ISDN with Frame Relay*, William Stallings, PHI.
2. *Communication Networks*, Leon Garcia widjaja, TMH, 2000.
3. *ATM Fundamentals*, N. N. Biswas, Adventure books publishers, 1998.

REFERENCES:

1. *High Performance TCP/IP Networking*, Mahbub Hassan, Raj Jain, PHI, 2005.
2. *ATM Networks*, Rainer Handel, Manfred N.Hubber, Stefan Schroder, Pearson Edu, 2002
3. *High Speed Networks and Internets,* William Stallings, Pearson edu., 2002

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3813) OPTICAL NETWORKS
(ELECTIVE II)

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

OPTICAL FIBER COMPONENTS: couplers, Isolators and Circulators, Multiplexers, Bragg grating, Fabry-perot Filters, Mach zender interfermometers, Arrayed waveguide grating, tunable filters, hi-channel count multiplexer architectures, optical amplifiers, direct and external modulation transmitters, pump sources for amplifiers, optical switching and wave length converters.

UNIT II

CLIENT LAYERS OF OPTICAL NETWORKS: SONET / SDH – Multiplexing, Frame Structure, Physical Layer, Infrastructure, ATM – Functions, Adaptation layers, QoS, Flow Control Signaling and Routing, IP – Routing, QoS, MPLS, Storage Area Networks – ESCON, Fiber Channel, HIPPI

UNIT III

WDM NETWORK ELEMENTS AND DESIGN: Optical Line Terminals and Amplifiers, Add/Drop Multiplexers, Optical Cross Connects, Cost tradeoffs in Network Design, LTD and RWA Problems, Dimensioning – Wavelength Routing Networks.

UNIT IV

NETWORK CONTROL, MANAGEMENT AND SURVIVABILITY: Network Management Functions, Optical Layer Services and Interfacing, Layers within Optical Layer, Multivendor Interoperability, Performance and Fault Management.

Basic Concepts of Survivability, Protection in SONET/SDH Links and Rings, Protection in IP Networks, Optical Layer Protection – Service Classes, Protection Schemes, Interworking between Layers.

UNIT V

ACCESS NETWORKS AND PHOTONIC PACKET SWITCHING: Network Architecture, Enhanced HFC, FTTC, Photonic Packet Switching – OTDM, Synchronization, Header Processing, Buffering, Burst Switching.

TEXT BOOKS:

1. *Optical Networks: A Practical Perspective*, Rajiv Ramaswami and Kumar N. Sivarajan, 2nd edition 2004, Elsevier Morgan Kaufmann Publishers (An Imprint of Elsevier).
2. *WDM Optical Networks: Concepts, Design and Algorithms*, C. Siva Rama Murthy and Mohan Guruswamy 2nd edition, 2003, PEI.
3. *Optical Networks*, Third Generation Transport Systems, Uyless Black, 2nd Ed., 2009,PEI.

REFERENCE BOOKS

1. *Optical Fiber Communications: Principles and Practice*- John.M.Senior, 2nd edition, 2000, PE.
2. *Fiber Optics Communication*, Harold Kolimbris, 2nd Ed., 2004, PEI.
3. *Networks*, Timothy S. Ramteke, 2 edition , 2004, PEI.
4. *Optical Fiber Communications*, Govind Agarwal, 2nd Ed., 2004, TMH.
5. *Optical Fiber Communications and Its Applications*, S.C.Gupta, 2004, PHI.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3814) COMPRESSION TECHNIQUES
(ELECTIVE II)

M.Tech I Year -II SEM (DECS)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

REVIEW OF INFORMATION THEORY: The discrete memory-less information source, Kraft inequality; optimal codes Source coding theorem. Compression Techniques, Lossless and Lossy Compression, Mathematical Preliminaries for Lossless Compression, Huffman Coding, Optimality of Huffman codes, Extended Huffman Coding, Adaptive Huffman Coding, Arithmetic Coding, Adaptive Arithmetic coding, Run Length Coding.

UNIT II

DICTIONARY TECHNIQUES: Static Dictionary, Adaptive Dictionary, LZ77, LZ78, LZW, Applications, Predictive Coding, Prediction with Partial Match, Burrows Wheeler Transform, Sequitur, Lossless Compression Standards (files, text, and images, faxes), Dynamic Markov Compression.

QUANTIZATION: Uniform & Non-uniform, optimal and adaptive quantization, vector quantization and structures for VQ, Optimality conditions for VQ, Predictive Coding, Differential Encoding Schemes

UNIT III

MATHEMATICAL PRELIMINARIES FOR LOSSY CODING: Rate distortion theory: Rate distortion function R(D),Properties of R(D); Calculation of R(D) for the binary source and the Gaussian source, Rate distortion theorem, Converse of the Rate distortion theorem.

UNIT IV

MATHEMATICAL PRELIMINARIES FOR TRANSFORMS: Karhunen Loeve Transform, Discrete Cosine and Sine Transforms, Discrete Walsh Hadamard Transform, Lapped transforms- Transform coding, Sub-band coding, Wavelet Based Compression, Analysis/Synthesis Schemes.

UNIT V

DATA COMPRESSION STANDARDS: Zip and Gzip, Speech Compression Standards: MPEG, JPEG 2000. MPEG, H264.

IMAGE COMPRESSION STANDARDS: Binary Image Compression Standards, Continuous Tone Still Image Compression Standards, Video Compression Standards.

TEXT BOOKS:

1. *Introduction to Data Compression,* Khalid Sayood, Morgan Kaufmann Publishers, 2nd edition, 2005.
2. *Data Compression: The Complete Reference* David Salomon, Springer Publications, 4th edition 2006.

3. *Elements of Information Theory*,Thomas M. Cover, Joy A. Thomas, John Wiley & Sons, Inc.,1991.

REFERENCES:

1. *Rate Distortion Theory: A Mathematical Basis for Data Compression* Toby Berger, Prentice Hall, Inc., 1971.
2. *The Transform and Data Compression Handbook*, K.R.Rao, P.C.Yip, CRC Press. 2001.
3. *Information Theory and Reliable Communication,* R.G.Gallager,John Wiley & Sons, Inc., 1968.
4. *Multi-resolution Signal Decomposition: Transforms, Subbands and Wavelets,* Ali N. Akansu, Richard A. Haddad,Academic Press. 1992
5. *Wavelets and Sub-band Coding,* Martin Vetterli, Jelena Kovacevic, Prentice Hall Inc., 1995.
6. *Digital Image Processing,* Rafael C. Gonzalez, Richard E. Woods, Pearson Education.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3815) DIGITAL SYSTEM DESIGN LAB

M.Tech I Year -II SEM (DECS)	**L**	**P**	**C**
	0	**4**	**2**

CYCLE 1:

1. Simulation and Verification of Logic Gates.
2.Design and Simulation of Half adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder and Full Adder.
3. Simulation and Verification of Decoder, MUXs, Encoder using all Modeling Styles.
4. Modeling of Flip-Flops with Synchronous and Asynchronous reset.
5. Design and Simulation of Counters-Ring Counter, Johnson Counter, and Up-Down Counter, Ripple Counter.
6. Design of a N-bit Register of Serial-in Serial-out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel Out.
7. Design of Sequence Detector (Finite State Machine-Mealy and Moore Machines).
8.4-Bit Multiplier, Divider. (for 4-Bit Operand)
9. Design ALU to Perform –ADD, SUB, AND-OR, 1‟s and 2‟s COMPLIMENT, Multiplication, Division.

CYCLE 2: After completing cycle 1,

Digital Circuit Description Using Verilog / VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
3. Synthesis of Digital Circuit.
4. Place and Router Techniques for FPGA‟s like Xilinx, Altera, Cypress, etc.,
5. Implementation of Design using FPGA and CPLD Devices.