R16

M.Tech - ES

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech EMBEDDED SYSTEMS (ES)

COURSE STRUCTURE

I Year – I Semester

S.No.	Course Code	Subject	L	T	P	CP
1.	16EC5501	Micro Controllers & Interfacing	4	-	-	4
2.	16EC5502	Embedded System Concepts	4	-	-	4
3.	16EC5503	Advanced Computer Architecture	4	-	-	4
4.	16EC5504	Advanced DSP & Applications	4	-	-	4
5.	16EC3801	Digital System Design	4	-	-	4
ELECTIVE- I						
6.	16EC5703	Digital IC Design	4	-	-	4
7.	16EC5701	VLSI Technology				
8.	16EC5710	Algorithms for VLSI Design Automation				
LABORATORY						
9.	16EC5505	Microcontrollers & Interfacing Lab	-	-	4	2
Contact periods / Week			24	-	4	**26**
			Total/Week **28**			

I Year – II Semester

S.No.	Course Code	Subject	L	T	P	CP
1.	16EC5506	Real Time Operating Systems	4	-	-	4
2.	16EC5507	Testing & Testability	4	-	-	4
3.	16EC5508	Hardware Software Co-Design	4	-	-	4
4.	16EC5509	Cryptography & Network Security	4	-	-	4
5.	16EC5708	FPGA Architecture and Applications	4	-	-	4
ELECTIVE II						
6.	16EC5510	Radio Frequency Identification	4	-	-	4
7.	16EC5511	Micro Electromechanical Systems				
8.	16EC5705	System Modeling & Simulation				
LABORATORY						
9.	16EC5512	RTOS and FPGA Lab	-	-	4	2
Contact Periods / Week			24	-	4	**26**
			Total/Week **28**			

II YEAR (III & IV Semesters)

S. No	Subject Code	Subject	Credits
1	16EC5513	Seminar	**2**
2	16EC5514	Project work	**16**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5501) MICRO CONTROLLERS & INTERFACING

M.Tech I Year -I SEM (ES)

L	T	C
4	-	4

UNIT I

INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, Addressing modes, Instruction set, Programming example,8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT II

MOTOROLA 68HC11:Controller features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system.

PIC MICROCONTROLLER:

Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, I2C bus, ADC, UART, PIC family parts.

UNIT III

MICROCONTROLLER INTERFACING: 8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing –Memory Management Unit, Instructions and data, cache memory Controller, On Chip Counters, Timers, Serial I/O Ports, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT-IV

ARM PROCESSOR FUNDAMENTALS:

Instruction Set, Registers, Timers, Pipeline and Memory Management.

UNIT V

INTERRUPT SYNCHRONIZATION:

Interrupt vectors & priority, external interrupt design. Serial I/O Devices: RS232 Specifications, RS552/Apple Talk/ RS 553/RS435 & other communication protocols. Serial Communication Controller.

CASE STUDIES:

Design of Embedded Systems using the micro controller 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

TEXT BOOKS:

1. *The 8051 Micro Controller & Embedded Systems Pearson Education, Asia (2000),*M.A. Mazadi & J.G. Mazidi.
2. *Designing with PIC Micro Controllers Pearson Education,* John B. Peatman,.
3. *Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999Jonathan* W. Valvano.
4. *ARM Systems Developer's Guides- Designing & Optimizing System Software*–Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCES:

1. *8-bit Embedded Controllers*, INTEL Corporation 1990.
2. *Designing with PIC Microcontrollers*, Pearson Education Inc, India, 2005. John B.Peatman,
3. *Embedded Microcomputer Systems, Real Time Interfacing*, Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5502) EMBEDDED SYSTEM CONCEPTS

M.Tech I Year -I SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems.

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication Interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT II

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space.

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging techniques.

UNIT III

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNITVI

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

UNIT V

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design.

DESIGN EXAMPLES: Telephone PBX, ink-jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1. *Computers as a component: principles of embedded computing system design*-wayne wolf.
2. *An embedded software premier*: David E. Simon.
3. *Embedded / real time systems*-KVKK Prasad, Dreamtech press, 2005.

REFERENCES:

1. *Embedded real time systems programming*-sri ram V Iyer, pankaj gupta, TMH, 2004.
2. *Embedded system design - A unified hardware/software introduction* - frank vahid, tony D.Givargis, John Willey, 2002.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5503) ADVANCED COMPUTER ARCHITECTURE

M.Tech I Year -I SEM (ES) **L T C**
4 - 4

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Elements of modern computers, Technology trends, cost-measuring and reporting performance quantitative principles of computer design.

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set, instructions for control flow, encoding an instruction set,the role of compiler.

UNIT II

INSTRUCTION LEVEL PARALLELISM (ILP): overcoming data hazards, reducing branch costs, high performance instruction delivery, and hardware based speculation, limitation of ILP.

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H/W support for more ILP at compile time , H/W verses S/W solutions.

UNIT III

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi-threading.

UNIT IV

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing an I/O system.

UNIT V

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster.

TEXT BOOKS:

1. *Computer Architecture A quantitative approach,* 3rd edition (An Imprint of Elsevier) John Hennessy & David A. Patterson Morgan Kufmann.

REFERENCES:

1. *Computer Architecture and parallel Processing,* International Edition McGraw-Hill. Kai Hwang and A. Briggs.
2. *Advanced Computer Architectures,* Pearson Dezso Sima, Terence Fountain, Peter Kacsuk.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5504) ADVANCED DSP & APPLICATIONS

M.Tech I Year -I SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Simple digital filters, Complementary Transfer Functions, Inverse Systems, System identification, Digital Two-Pairs, Algebraic Stability Test.

DIGITAL FILTER STRUCTURE AND DESIGN: All pass filters, Tunable IIR Digital filter, IIR tapped Cascaded Lattice Structures, FIR Cascaded lattice Structures, Parallel All pass realization of IIR Transfer Functions, State Space Structures, Polyphase Structures, Digital Sine- Cosine generator.

UNIT II

Computational Complexity of Digital filter Structures, Design of IIR filter using pade approximation, Least square design methods, Design of computationally Efficient FIR Filters.

UNIT III

DSP ALGORITHMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT IV

ANALYSIS OF FINITE WORD LENGTH EFFECTS: The Quantization Process and errors, Quantization of fixed-point Numbers, Analysis of Coefficient quantization effects, A/D conversion Noise Analysis, Analysis of Arithmetic Round of errors, Dynamic range scaling, Signal to Noise ratio in Low-order IIR Filters, Low sensitivity Digital filters, Reduction of Product Round off Errors using error feedback, Limit cycle in IIR Digital filters, Round of errors in FFT algorithms.

UNIT V

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Nonstationary Signals, Musical Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete –Time Analytic Signal generation.

MULTIRATE SIGNAL PROCESSING:

Decimation factor, Interpolation factor, Sampling rate, conversion by rational factor I/D, Filter Design & Implementation for sampling rate conversion.

TEXT BOOKS:

1. *Digital Signal Processing*, by Sanjit K Mitra, Tata McGraw Hill Publications.
2. *Digital Signal Processing Principles, Algorithms, Applications*, by J G Proakis, D G Manolokis, PHI.

REFERENCES:

1. *Discrete-Time Signal Processing*, by A V Oppenhiem, R W Schafer, Pearson Education.
2. *DSP-A Practical Approach-Emmanuel* ,C Ifeacher Barrie. W. Jervis, Pearson Education.
3. *Modern spectral Estimation techniques*, by S.M.Kay, PHI, 1997.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3801) DIGITAL SYSTEM DESIGN

M.Tech I Year -I SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, Design of sequential circuits using ROMs, PLAs, CPLD and FPGAs

UNIT II

FAULT MODELING: Fault classes and models – Stuck at faults, Bridging faults, Transition and Intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods– Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT III

TEST PATTERN GENERATION: D – Algorithm, PODEM, Random testing, Transition count testing, Signature Analysis and Testing for bridging faults.

UNIT IV

PROGRAMMING LOGIC ARRAYS: Introduction, Design using PLA's, PLA minimization and PLA folding.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and Fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT V

PLA TESTING: Fault models, Test generation and Testable PLA design.

ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, Flow table, State reduction, Minimal closed covers, Races, Cycles and Hazards.

TEXTBOOKS:

1. *Switching & finite Automata Theory,* Z. Kohavi , (TMH)
2. *Logic Design Theory,* N. N. Biswas,– (PHI)
3. *Digital Logic Design Principles,* Nolman Balabanian, Bradley Calson Wily Student Edition 2004.

REFERENCES:

1. *Digital System Testing and Testable Design,* M. Abramovici, M. A. Breues, A. D. Friedman, Jaico Publications.
2. *Fundamentals of Logic Design,* Charles H. Roth Jr.
3. *Computer Aided Logic Design,* Frederick. J. Hill & Peterson, Wiley 4th Edition.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5703) DIGITAL IC DESIGN

M.Tech I Year -I SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

CMOS inverters -static and dynamic characteristics. Static and Dynamic CMOS design- Domino and NOR logic - combinational and sequential circuits.

UNIT II

Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design. Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifters - CMOS memory design - SRAM and DRAM.

UNIT III

Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

UNIT IV

LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT V

SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1. *CMOS Digital Integrated Circuits - Analysis & Design,* 1999SungMo Kang & Yusuf Leblebici, MGH, Second Ed.
2. *Digital Integrated Circuits - A Design Perspective*, Prentice Hall, 1997.
3. *Introduction to VLSI Design,* Jan M Rabaey Eugene D Fabricus McGraw Hill International Edition.1990.

REFERENCES:

1. *Digital Integrated Circuit Design,* Ken Martin Oxford University Press, 2000.
2. *Principles of CMOS VLSI Design: A System Perspective*, Addision-Wesley 2nd Edition, 2002Neil H E West and Kamran Eshranghian.
3. *CMOS circuit design, layout, and simulation,* R. J. Baker, H. W. Li, and D. E. Boyce New York: IEEE Press, 1998.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5701) VLSI TECHNOLOGY

M.Tech I Year -I SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BiCOMS CIRCUITS: I_{ds} - V_{ds} Relationships, Threshold Voltage V_t ,g_m, g_{ds} and ω_o, Pass Transistor, MOS,CMOS & Bi-CMOS Inverters, $Z_{p.u}/Z_{p.d}$, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT IV

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT V

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing, Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:

1. *Essentials of VLSI Circuits and Systems*, K. Eshraghian et.al (3 authors) PHI of India Ltd., 2005.
2. *Modern VLSI Design*, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. *Principals of CMOS Design*.N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. *Introduction to VLSI Design* , Fabricius, MGH International Edition, 1990.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5710) ALGORITHM FOR VLSI DESIGN AUTOMATION

M.Tech I Year -I SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT II

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

UNIT IV

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXT BOOKS:

1. *Algorithms for VLSI Design Automation*, Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.S.H.Gerez,
2. *Algorithms for VLSI Physical Design Automation*, Naveed Sherwani Springer International 3rd edition.

REFERENCES:

1. *Computer Aided Logical Design with Emphasis on VLSI*, Hill & Peterson Wiley, 1993,
2. *Modern VLSI Design: Systems on silicon*, Wayne Wolf Pearson Education Asia, 2nd Edition, 199**8.**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5505) MICROCONTROLLERS AND INTERFACING LAB

M.Tech I Year -I SEM (ES) **L T C**
0 4 2

A) ASSEMBLY:

1. Write a program to calculate the 500 us time delay.
2. Write a program to toggle the LEDs with the 5 sec time delay.
3. Write a program to transmit and receive the data through serial port.

B) PROGRAMING IN EMBEDDED C:

Use 89C51 Development board/equivalent for the following Experiments using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 ms delay.
2. Program to display a given string on LCD using interrupt.

Use ARM Microcontroller for the following Experiments.

1. Program to transmit & receive a message from µC to PC serially using RS232.
2. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
3. Generation of PWM signal.

C) ARM INTERFACING:

1. 8 bit LED and Switch interface.
2. Buzzer, Relay and Stepper motor interface.
3. 4x4 Key Board and display Interface.
4. Traffic light controller.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5506) REAL TIME OPERATING SYSTEMS

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

OPERATING SYSTEMS:

Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT II

INTRODUCTION TO UNIX:

Overview of Commands, File I/O (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT III

REAL TIME SYSTEMS: Definition of RTOS**,** Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources.

UNIT IV

APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs Static Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

INTER PROCESS COMMUNICATION: Inter process communication & synchronization of process, tasks and threads, multiple process in an application, problem of sharing data by multiple tasks and routines.

UNIT V

CASE STUDIES-VX WORKS: Memory Managements, Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting, Watch Dogs, I/O System.

RT Linux: Process Management, Interrupt Management, Embedded LINUX, Basic concepts of Android OS.

TEXT BOOKS:

1. *Advanced Unix Programming*, Richard Stevens.
2. *Real Time Systems*, Jane W.S. Liu Pearson Education.
3. *Real Time Systems*, C.M.Krishna, KANG G. Shin, McGraw. Hill.

REFERENCES:

1. Vx Works Programmers Guide.
2. www.tidp.org

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5507) TESTING AND TESTABILITY

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models, Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For SSFs in Combinational and Sequential Circuits, Functional Testing With Specific Fault Models.

UNIT III

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques, Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design, Board Level and System Level DFT Approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT IV

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT V

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model, Memory Test Requirements for MBIST.

BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. *Digital Systems Testing and Testable Design*, Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Jaico Publishing House, 2001.

REFERENCES:

1. *Design for Test for Digital ICs & Embedded Core Systems*, Alfred Crouch, Prentice Hall.
2. *Introduction to VLSI Testing, Prentice Hall*, Englehood Cliffs, 1998. Robert J.Feugate, Jr., Steven M.Mentyn.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5508) HARDWARE SOFTWARE CODESIGN

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
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UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: Hardware-software partitioning distributed system co-synthesis.

UNIT II

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60),Mixed Systems.

UNIT III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT IV

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating, concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT V

LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages.

LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II:

Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1. *Hardware / software co- design Principles and Practice,* 2009, Springer, Jorgen Staunstrup, Wayne Wolf.

2. *Hardware / software co- design Principles and Practice*, 2002, kluwer academic Publishers.

REFERENCES:

1. *Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform,* 1st Edition. Naim Dahnoun.

2. *Digital Signal Processing-A Student Guide* T.J. Terrel and Lik-Kwan Shark, 1st Edition, Macmillan press ltd.

3. *Digital Signal Processing: A System Design Approach*,David J Defatta J, Lucas Joseph G & Hodkiss William S, 1st Edition, John Wiley.

4. *DSP Applications using 'C' and the TMS320C6X* ,DSK Rulph Chassaing, 1st Edition.

5. *Digital Signal Processing Design*, 1st Edition Andrew Bateman, Warren Yates.

6. Digital Signal Processing, 1st Edition, PH. Oppenheim A.V and Schafer R.W.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5509) CRYPTOGRAPHY AND NETWORK SECURITY

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

SYMMETRIC CIPHERS: Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS: Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT II

NETWORK SECURITY PRACTICE: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT III

SYSTEM SECURITY: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

WIRELESS SECURITY: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT IV

SECURE NETWORKING THREATS: Attack Process, Attacker Types, Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

ENCRYPTION TECHNIQUES: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT V

DESIGNING SECURE NETWORKS: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies, General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. *Cryptography and Network Security – Principles And Practices*, Pearson Education, 3rd Edition, 2003. William Stallings.
2. *Network Security Architectures*, Published by Cisco Press, First Ed. 2004. Sean Convery.

REFERENCES:

1. *Cryptography and Network Security*, Tata McGraw Hill, 2003. Atul Kahate.
2. *Applied Cryptography*, John Wiley and Sons Inc, 2001. Bruce Schneier.
3. *Wi-Fi Security*, McGraw Hill, 2003. Stewart S. Miller.
4. *Security In Computing*, 3rd Edition, Pearson Education, 2003. Charles B. Pfleeger, Shari Lawrence Pfleeger.
5. *Inside Internet Security*, Addison Wesley, 2005, Jeff Crume.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5708) FPGA ARCHITECTURE AND APPLICATIONS

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
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UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5), Cypres FLASH 370 Device Technology, Lattice PLSI's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Programming technologies, Logic Blocks, Routing Architecture, Design Flow, Technology Mapping for FPGAs.

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array),ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT III

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs, Problem of Initial State Assignment for One Hot Encoding, Derivations of State Machine Charges.

REALIZATION OF STATE MACHINE: Charts with a PAL, Alternative Realization for State Machine Chart using Microprogramming, Linked State Machines, One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties, Extended Petrinetes for Parallel Controllers, Finite State Machine Case study, metastability, synchronization

UNIT IV

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs, State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One – Hot Design, K Application of One – Hot Method, System Level Design – Controller, Data Path and Functional Partition.

UNIT V

CASE STUDIES: Combinational Logic Circuits - Parallel Adder Cell, Parallel Adder Sequential Circuits - Decade Counters, Multipliers, Parallel Controller design.

TEXT BOOKS/ REFERENCES:

1. *Digital Design Using Field Programmable Gate Array*, jPrentice Hall (Pte), 1994. P.K.Chan & S. Mourad.
2. *Field Programmable Gate Array Technology*, Kluwer Academic Publicatgions,1994. S.Trimberger, Edr.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5510) RADIO FREQUENCY IDENTIFICATION
(ELECTIVE II)

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

UNDERSTANDING RFID TECHNOLOGY: Introduction, RFID Technology, The Elements of an RFID system, Coupling, Range, and Penetration, RFID Applications, VeriChip and Mark of the Beast.

UNIT II

A HISTORY OF THE EPC: Introduction, The Distributed Intelligent Systems Center, Meanwhile, at Procter & Gamble, "Low-Cost" RFID Protocols, "Low-cost" Manufacturing, The Software and the Network, Privacy, Harnessing the Juggernaut, The Six Auto-ID Labs, The Evolution of the Industry, The Creation of EPC global.

UNIT III

RFID SOLUTION INFRASTRUCTURE: Different kinds of RFID systems, basic configuration of RFID solutions, RFID middleware, Application servers and client integration, RFID standards on Electronic Product Coding (EPC) and Physical Markup Language (PML); information network, integration with enterprise applications

UNIT IV

RFID, PRIVACY, AND REGULATION: Introduction, Understanding RFID‟s Privacy Threats, RFID and the United States Regulatory Landscape: Introduction, Current State of RFID Policy, Individuals, Business, Government, Miscellaneous, Integrity and Security of the System, Government Access, Health Impact, Labor Impact.

UNIT V

APPLICATIONS: Object identification and tracking, transforming the Battlefield with RFID, Logistics and the Military, RFID in the Pharmacy, CVS and Auto-ID, Project Jump Start, RFID in the Store.

TEXT BOOKS:

1. *RFID Applications, Security, and privacy,* Pearson Education. Simson Garfinkel and Beth Rosenberg.
2. *Radio Frequency Identification,* First edition, McGraw-Hill Professional. Steven Shepard.
3. *RFID Field Guide: Deploying RFID Systems*. Sun Microsystems Press, Prentice Hall Professional Technical Reference. Bhuptani, M, and Moradpour.

REFERENCES:

1. *RFID technologies: supply-chain applications and implementation issues,* Angeles, R
2. *Integrating the supply chain with RFID: a technical and business analysis,* Asif, Z, Mandviwalla, M.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5511) MICRO ELECTROMECHANICAL SYSTEMS
(ELECTIVE II)

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
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UNIT I

INTRODUCTION, BASIC STRUCTURES OF MEM DEVICES: (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro Electromechanical Systems (MEMs) to Mechanical (force, pressure etc.) Thermal,Electrical, Optical and Magnetic stimuli, Compatability of MEMS from the point of Power Dissipation, Leakage etc.

UNIT II

REVIEW OF MECHANICAL CONCEPTS: Stress, Strain, Bending Moment, Deflection Curve, Differential Equations Describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed Beam, Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes, Deflection with Voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT III

TWO TERMINAL MEMS: Capacitance Vs Voltage Curve – Variable Capacitor, Applications of Variable Capacitors, Two Terminal MEM Structures, Three Terminal MEM Structures – Controlled Variable Capacitors, MEM as a Switch and Possible Applications.

UNIT IV

MEM CIRCUITS & STRUCTURES FOR SIMPLE GATES: AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT V

MEM TECHNOLOGIES: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc., Etching Technologies, Metal Based MEMS: Thin and Thick Film Technologies for MEMS. Process flow and Description of the Processes.Status of MEMS in the Current Electronics scenario.

TEXT BOOKS:

1. *R.F. MEMS Theory, Design and Technology*, John Wiley & Sons, 2003. Gabriel.M.Review.
2. *Strength of Materials*, CBS Publishers & Distributors., 2000. Thimo Shenko.
3. *Sensor Technology and Devices*, Artech House, London 1994. Ristic L. (Ed.).
4. *MEMS and NEMS, Systems Devices and Structures*,CRC Press,2002.Servey E.Lyshevski.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5705) SYSTEM MODELLING & SIMULATION
(ELECTIVE II)

M.Tech I Year -II SEM (ES)

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UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT II

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT III

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

MARKOV PROCESS: Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT IV

EVENT DRIVEN MODELS: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

UNIT V

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1.*System Modeling & Simulation, an Introduction*, Frank L. Severance, John Wiley & Sons, 2001.
2.*Simulation Modeling and Analysis,* Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFERENCES:

1.*Systems Simulation*, Geoffery Gordon, PHI, 1978.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5512) RTOS AND FPGA LAB

M.Tech I Year -II SEM (ES)	**L**	**T**	**C**
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1. RTOS System solution & tools.
2. Testing RTOS Environment and System Programming
   a) Keil Tools
   b) RTOS System Solutions with Tornado tools.
3. Embedded DSP based System Designing
   a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
   b) Analog DSP tool kit.
4. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after Simulation are to be verified using FPGA/CPLD blocks from different commercially available products on:
   a) Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
   b) Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

Required Software Tools for FPGA:

1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and above)
2. Xilinx 9.1i and above for FPGA/CPLDS / FPGA Advantage.