SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech (VLSI)
COURSE STRUCTURE

I Year – I Semester

S.No.	Course code	Subject	L	T	P	CP
1.	16EC5701	VLSI Technology	4	0	-	4
2.	16EC5702	Analog IC Design	4	0	-	4
3.	16EC5703	Digital IC Design	4	0	-	4
4.	16EC5704	Verilog HDL	4	0	-	4
5.	16EC5508	Hardware Software Co-Design	4	0	-	4
ELECTIVE-I						
6.	16EC5502	Embedded system Concepts	4	0	-	4
7.	16EC5705	System Modeling & Simulation				
8.	16EC5706	ASIC Design				
LABORATORY						
9.	16EC5707	Digital IC Design Lab	-	-	4	2
Contact periods / week			24	0	4	26
			Total/Week 28			

I Year – II Semester

S.No.	Course code	Subject	L	T	P	CP
1.	16EC5708	FPGA Architectures & Applications	4	0	-	4
2.	16EC5507	Testing & Testability	4	0	-	4
3.	16EC5709	Low Power VLSI Design	4	0	-	4
4.	16EC5710	Algorithms for VLSI Design Automation	4	0	-	4
5.	16EC5711	Scripting Language for VLSI Design Automation	4	0	-	4
ELECTIVE- II						
6.	16EC5712	Nano Electronics	4	0	-	4
7.	16EC5509	Cryptography & Network Security				
8.	16EC5506	Real Time Operating Systems				
LABORATORY 1						
9.	16EC5713	Mixed Signal Lab	-	-	4	2
Contact Periods / Week			24	0	4	26
			Total/Week 28			

II YEAR (III & IV Semesters)

S. No	Subject Code	Subject	Credits
1	16EC5714	Seminar	2
2	16EC5715	Project work	16

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5701) VLSI TECHNOLOGY

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BiCOMS CIRCUITS: I_{ds} - V_{ds} Relationships, Threshold Voltage V_t, g_m, g_{ds} and ω_o, Pass Transistor, MOS,CMOS & Bi-CMOS Inverters, $Z_{p.u}/Z_{p.d}$, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, wires and vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT IV

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT V

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing, Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:

1. *Essentials of VLSI Circuits and Systems*, K. Eshraghian et.al(3 authors) PHI of India Ltd.,2005.
2. *Modern VLSI Design*, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. *Principals of CMOS Design*, N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. *Introduction to VLSI Design*, Fabricius, MGH International Edition, 1990.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5702) ANALOG IC DESIGN

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR: MOS transistors- modeling in linear, saturation and cut off high frequency equivalent circuit. Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers, Simple CMOS Current Mirror, High Output Impedance Current Mirrors and Bipolar Gain Stages, Frequency Response.

UNIT II

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOS Operational Amplifier, Feedback and Operational Amplifier Compensation, Advanced Current Mirror, Common Mode Feedback Circuits, Current Feedback Operational Amplifier, Comparator , Charge Injection Error, Latched Comparator and Bi-CMOS Comparators.

UNIT III

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits, Switched Capacitor Circuits, Basic Operation and Analysis. First Order and Biquard Filters.

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-II: Charge Injection. Switched Capacitor Gain Circuit, Correlated, Double Sampling Techniques, Other Switched Capacitor Circuits.

UNIT IV

DATA CONVERTERS: Ideal D/A & A/D Converters, Quantization Noise, Performance Limitations, Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating, Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT V

OVER SAMPLING CONVERTERS AND FILTERS: Over Sampling With and Without Noise Shaping, Digital Decimation Filter, High Order Modulators, Band Pass over Sampling Converter, Practical Considerations, And Continuous Time Filters.

TEXT BOOKS:

1. *Analog Integrated Circuit Design*, D.A.JOHN & KEN MARTIN, John Wiley, 1997.
2. *Design of Analog CMOS Integrated Circuit*, Behzad Razavi, Tata-Mc GrawHill, 2002.

REFERENCES:

1. *CMOS Analog Circuit Design*, Philip Allen & Douglas Holberg, Oxford University Press, 2002.
2. *Analog MOS Integrated Circuits*, John Wiley, 1986.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5703) DIGITAL IC DESIGN

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

CMOS inverters -static and dynamic characteristics, Static and dynamic CMOS design-domino and NORA logic - combinational and sequential circuits.

UNIT II

Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design, Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter - CMOS memory design - SRAM and DRAM

UNIT III

Bipolar gate Design- BiCMOS logic - static and dynamic behavior -Delay and power consumption in BiCMOS Logic.

UNIT IV

LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT V

SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1. *CMOS Digital Integrated Circuits - Analysis & Design*-Sung-Mo Kang & Yusuf Leblebici, MGH, Second Ed., 1999.
2. *Digital Integrated Circuits - A Design Perspective,* Jan M Rabaey, Prentice Hall, 1997.
3. *Introduction to VLSI Design* , Eugene D Fabricus, McGraw Hill International Edition.1990.

REFERENCES:

1. *Digital Integrated Circuit Design,* Ken Martin, Oxford University Press, 2000.
2. *Principles of CMOS VLSI Design - A System Perspective,* Neil H E West and Kamran Eshranghian, Addision-Wesley 2nd Edition,2002.
3. *CMOS circuit design, layout, and simulation,* R. J. Baker, H. W. Li, and D. E. Boyce, New York: IEEE Press, 1998.
4. *Analysis and Design of Digital Integrated Circuits,* David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Third Edition, McGraw-Hill, 2004.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5704) VERILOG HDL

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL: User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings, Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay: Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Synthesis of Sequential Logic: Synthesis of Sequential UDPs, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines.

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined

Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT V

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates, Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic, Design Examples in Verilog.

TEXT BOOKS:

1. *Modeling, Synthesis and Rapid Prototyping with the Verilog HDL*, M.D.CILETTI, Prentice-Hall, 1999.
2. *VHDL Analysis and Modeling of Digital Systems*, Z.NAWABI, (2/E), McGraw Hill, 1998.

REFERENCES:

1. *Verilog Digital – Computer Design*, M.G.ARNOLD, Prentice-Hall (PTR), 1999.
2. *VHDL*, PERRY, (3/E), McGraw Hill.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5508) HARDWARE SOFTWARE CO- DESIGN

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware-software partitioning distributed system co-synthesis.

UNIT II

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT IV

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT V

LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages,

LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the COSYMA system and LYCOS system.

TEXT BOOKS:

1.*Hardware / software co- design Principles and Practice,* 2009, Springer, Jorgen Staunstrup, Wayne Wolf.

2. *Hardware / software co- design Principles and Practice,* 2002, kluwer academic Publishers.

REFERENCES:

1. *Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform,* 1st Edition. Naim Dahnoun.

2. *Digital Signal Processing-A Student Guide* T.J. Terrel and Lik-Kwan Shark, 1st Edition, Macmillan press ltd.

3. *Digital Signal Processing: A System Design Approach*,David J Defatta J, Lucas Joseph G & Hodkiss William S, 1st Edition, John Wiley.

4. *DSP Applications using 'C' and the TMS320C6X* ,DSK Rulph Chassaing, 1st Edition.

5. *Digital Signal Processing Design*, 1st Edition Andrew Bateman, Warren Yates.

6. Digital Signal Processing, 1st Edition, PH. Oppenheim A.V and Schafer R.W.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5502) EMBEDDED SYSTEM CONCEPTS
(ELECTIVE I)

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication Interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT II

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT III

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

UNIT IV

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

UNIT V

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1.Computers as a component: principles of embedded computing system design-wayne wolf
2.An embedded software premier: David E. Simon
3.Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1.Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2. Embedded system design - A unified hardware/software introduction - frank vahid, tony D.Givargis, John Willey, 2002

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5705) SYSTEM MODELLING & SIMULATION
(ELECTIVE I)

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT II

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT III

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

MARKOV PROCESS: Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT IV

EVENT DRIVEN MODELS: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

UNIT V

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1. *System Modeling & Simulation, an Introduction*, Frank L. Severance, John Wiley & Sons, 2001.
2. *Simulation Modeling and Analysis*, Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFERENCES:

1. *Systems Simulation*, Geoffrey Gordon, PHI, 1978.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5706) ASIC DESIGN
(ELECTIVE I)

M.Tech I Year -I Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

ASIC DESIGN STYLES: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

ASICS – PROGRAMMABLE LOGIC DEVICES: Overview – PAL –based PLDs: Structures, PAL Characteristics – FPGAs: Introduction, selected families – design outline.

UNIT II

ASICS –DESIGN ISSUES: Design methodologies and design tools – design for testability – economies.

ASIC CHARACTERISTICS AND PERFORMANCE: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT III

ASICS-DESIGN TECHNIQUES: Overview- Design flow and methodology-Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

UNIT IV

LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and logic synthesis - VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation-automatic test pattern generation.

UNIT V

ASIC CONSTRUCTION: Floor planning, placement and routing system partition.

FPGA PARTITIONING: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

TEXT BOOKS:

1. *Integrated circuit engineering*, L.J.Herbst, OXFORD SCIENCE Publications, 1996.

REFERENCES:

1. *Application -Specific integrated circuits*, M.J.S.Smith, Addison-Wesley Longman Inc 1997.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5707) DIGITAL IC DESIGN LAB

M.Tech I Year -I Sem. (VLSI)	**L**	**P**	**C**
	0	**4**	**2**

1. Digital Circuits Description using Verilog and VHDL.
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

NOTE: Required Software Tools:
1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 11.1i and Above for FPGA/CPLDS / FPGA Advantage.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5708) FPGA ARCHITECTURE & APPLICATIONS

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice PLSI's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Programming technologies, Logic Blocks, Routing Architecture, Design Flow, Technology Mapping for FPGAs.

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT III

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs, Problem of Initial State Assignment for One Hot Encoding, Derivations of State Machine Charges.

REALIZATION OF STATE MACHINE: Charts with a PAL, Alternative Realization for State Machine Chart using Microprogramming, Linked State Machines. One – Hot State Machine, Petrinets for State Machines – Basic Concepts, Properties, Extended Petrinets for Parallel Controllers. Finite State Machine Case study, meta stability, synchronization

UNIT IV

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One – Hot Design, Application of One – Hot Method, System Level Design – Controller, Data Path and Functional Partition.

UNIT V

CASE STUDIES: Combinational Logic Circuits - Parallel Adder Cell, Parallel Adder Sequential Circuits - Decade Counters, Multipliers, Parallel Controller design.

TEXT BOOKS/ REFERENCES:

1. *Digital Design Using Field Programmable Gate Array*, P.K.Chan & S. Mourad, jPrentice Hall (Pte), 1994.
2. *Field Programmable Gate Array Technology*, S.Trimberger, Edr., Kluwer Academic Publicatgions,1994.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5507) TESTING & TESTABILITY

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models, Levels of Modeling, Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For SSFs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models..

UNIT III

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques, Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design, Board Level and System Level DFT Approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT IV

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT V

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. *Digital Systems Testing and Testable Design*, Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Jaico Publishing House, 2001.

REFERENCES:

1. *Design for Test for Digital ICs & Embedded Core Systems*, Alfred Crouch, Prentice Hall.
2. *Introduction to VLSI Testing, Prentice Hall*, Englehood Cliffs, 1998. Robert J.Feugate, Jr., Steven M.Mentyn,

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(16EC5709) LOW POWER VLSI DESIGN

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT II

LOW-VOLTAGE/LOW POWER CMOS/ BiCMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models, Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT III

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits, ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT IV

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT V

SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1. *CMOS/BiCMOS ULSI low voltage, low power*, Yeo Rofail/ Gohl(3 Authors), Pearson Education Asia 1st Indian reprint,2002.
2. *Practical Low Power Digital VLSI Design*, Gary K. Yeap, KAP, 2002.

REFERENCES:

1. *Basic VLSI Design,* Douglas A.Pucknell & Kamran Eshraghian, 3rd edition PHI.
2. *Digital Integrated circuits*, J.Rabaey, PH,1996.
3. *CMOS Digital ICs*, Sung-mo Kang and yusuf leblebici, 3rd edition TMH 2003.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5710) ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE I)

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT II

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT IV

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. *Algorithms for VLSI Design Automation*, S.H.Gerez, Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. *Algorithms for VLSI Physical Design Automation*, Naveed Sherwani, 3rd edition, Springer International Edition, 2005.

REFERENCES:

1. *Computer Aided Logical Design with Emphasis on VLSI*, Hill & Peterson, Wiley, 1993.
2. *Modern VLSI Design: Systems on silicon*, Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5711) SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
	4	**-**	**4**

UNIT I
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT II
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT III
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT IV
Debugger Internal & Externals Portable Functions, Extensive Exercises for Programming in PERL

UNIT V
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

TEXT BOOKS:
1. *Learning PERL*, Randal L, Schwartz Tom Phoenix, Oreilly Publications, 3rd Edn.,2000.
2. *Programming PERL*, Larry Wall, Tom Christiansen, John Orwant, Oreilly Publications, 3rd Edn., 2000.
3. *PERL Cookbook*, Tom Christiansen, Nathan Torkington, Oreilly Publications, 3rd Edn,2000.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5712) NANO ELECTRONICS
(ELECTIVE II)

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
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UNIT I

TECHNOLOGY AND ANALYSIS:

Film Deposition Methods, Lithography, Material Removing Technologies, Etching and Chemical, Mechanical Processing, Scanning Probe Techniques.

CARBON NANO STRUCTURES: Carbon Clusters, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT II

LOGIC DEVICES: Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT III

RADOM ACESS MEMORIES: High Permitivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT IV

MASS STORAGE DEVICES:

Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT V

DATA TRANSIMISSION, INTERFACES AND DISPLAYS:

Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:

1. *Nano Electronics and Information Technology*, Rainer Waser, Wiley VCH, April 2003.
2. *Introduction to Nano Technology*, Charles Poole, Wiley Interscience, May 2003.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5509) CRYPTOGRAPHY & NETWORK SECURITY
(ELECTIVE II)

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
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UNIT I

SYMMETRIC CIPHERS: Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS: Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT II

NETWORK SECURITY PRACTICE: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT III

SYSTEM SECURITY: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

WIRELESS SECURITY: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT IV

SECURE NETWORKING THREATS: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

ENCRYPTION TECHNIQUES: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT V

DESIGNING SECURE NETWORKS: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security

Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. *Cryptography and Network Security, Principles and Practices*-William Stallings, Pearson Education, 3rd Edition, 2003.
2. *Network Security Architectures*, Sean Convery, Published by Cisco Press, First Ed. 2004.

REFERENCES:

1. *Cryptography and Network Security*, Atul Kahate, Tata McGraw Hill, 2003.
2. *Applied Cryptography*, Bruce Schneier, John Wiley and Sons Inc, 2001.
3. *Wi-Fi Security*, Stewart S. Miller, McGraw Hill, 2003.
4. *Security In Computing*, Charles B. Pfleeger, Shari Lawrence Pfleeger, 3rd Edition, Pearson Education, 2003.
5. *Inside Internet Security*, Jeff Crume, Addison Wesley, 2005.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5506) REAL TIME OPERATING SYSTEMS
(ELECTIVE II)

M.Tech I Year -II Sem. (VLSI)	**L**	**T**	**C**
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UNIT I
OPERATING SYSTEMS
Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel, Capabilities of Commercial Real Time Operating Systems.

UNIT II
INTRODUCTION TO UNIX
Overview of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT III
REAL TIME SYSTEMS: Definition of RTOS**,** Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources.

UNIT IV
APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs Static Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.
INTER PROCESS COMMUNICATION: Inter process communication & synchronization of process , tasks and threads, multiple process in an application , problem of sharing data by multiple tasks and routines.

UNIT V
CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System.
RT Linux: Process Management, Interrupt Management, Embedded LINUX, Basic concepts of Android OS.

TEXT BOOKS:
1. *Advanced Unix Programming*, Richard Stevens.
2. *Real Time Systems*, Jane W.S. Liu, Pearson Education.
3. *Real Time System*, C.M.Krishna, KANG G. Shin, McGraw. Hill.

REFERENCES:

1. Vx Works Programmers Guide
2. www.tidp.org

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC5713) MIXED SIGNAL LABORATORY

M.Tech I Year -II Sem. (VLSI)	**L**	**P**	**C**
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1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

NOTE: Required Software Tools:
1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.