### I Year – I Semester

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16EC3801</td>
<td>Digital System Design</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>16EC3802</td>
<td>Advanced Digital Signal Processing</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>16EC3803</td>
<td>Digital Communication Techniques</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>16EC3804</td>
<td>Adaptive Signal Processing</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>16EC5502</td>
<td>Embedded System Concepts</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
</tbody>
</table>

#### ELECTIVE I

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>16EC5503</td>
<td>Advanced Computer Architectures</td>
<td>4</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>16EC3805</td>
<td>DSP Processors &amp; Architectures</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>16EC5709</td>
<td>Low Power VLSI Design</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### LABORATORY

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>16EC3806</td>
<td>Communications &amp; Signal Processing Lab</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
</tbody>
</table>

Contact periods / week: 24 - 4 = 26

Total/Week: 28

### I Year – II Semester

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16EC3807</td>
<td>Micro Computer System Design</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>16EC3808</td>
<td>Image &amp; Video Processing</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>16EC3809</td>
<td>Wireless Communications</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>16EC3810</td>
<td>Coding Theory &amp; Techniques</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>16EC3811</td>
<td>Detection &amp; Estimation of Signals</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
</tbody>
</table>

#### ELECTIVE II

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>16EC3812</td>
<td>Hi-Speed Networks</td>
<td>4</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>16EC3813</td>
<td>Optical Networks</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>16EC3814</td>
<td>Compression Techniques</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### LABORATORY

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>16EC3815</td>
<td>Digital System Design Lab</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
</tbody>
</table>

Contact Periods / Week: 24 - 4 = 26

Total/Week: 28

### II YEAR  (III & IV Semesters)

<table>
<thead>
<tr>
<th>S.No</th>
<th>Subject Code</th>
<th>Subject</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16EC3816</td>
<td>Seminar</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>16EC3817</td>
<td>Project work</td>
<td>16</td>
</tr>
</tbody>
</table>
UNIT I
DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.
SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, Design of sequential circuits using ROMs, PLAs, CPLD and FPGAs

UNIT II
FAULT MODELING: Fault classes and models – Stuck at faults, Bridging faults, Transition and Intermittent faults.
TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods– Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT III
TEST PATTERN GENERATION: D – Algorithm, PODEM, Random testing, Transition count testing, Signature Analysis and Testing for bridging faults.

UNIT IV
PROGRAMMING LOGIC ARRAYS: Introduction, Design using PLA’s, PLA minimization and PLA folding.

UNIT V
PLA TESTING: Fault models, Test generation and Testable PLA design.
ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, Flow table, State reduction, Minimal closed covers, Races, Cycles and Hazards.

TEXTBOOKS:
2. *Logic Design Theory*, N. N. Biswas,– (PHI)

REFERENCES:
UNIT I
LTI SYSTEMS: Types of Linear-Phase transfer functions, Simple Digital Filters, Complementary Transfer Function, Inverse Systems, System Identification, Digital Two-Pairs, Algebraic Stability Test.

UNIT II

UNIT III
MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT IV
POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.
PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT V
ANALYSIS OF FINITE WORDLENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS: Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality-Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

REFERENCES:
UNIT I

UNIT II
COMMUNICATION OVER ADDITIVE GAUSSIAN NOISE CHANNELS : Optimum receiver for signals corrupted by additive white Gaussian noise (AWGN)- Cross correlation demodulation, matched filter demodulator and error probabilities.
Optimum receiver for signals with random phase in AWGN channels, Optimum receiver for binary signals, Optimum receiver for M-array orthogonal signals, Probability of error for envelope detection of Mary orthogonal signals. Optimum waveform receiver for colored Gaussian noise channels, Karhunen-Loeve expansion approach, and whitening.

UNIT III
FADING CHANNELS: Characterization of fading multipath channels, Statistical Models for fading channels, Time varying Channel impulse response, narrow and wide band fading models, channel correlation functions, Key multipath parameters, Rayleigh and Ricean fading channels, Simulation methodology of fading channels.

UNIT IV
DIGITAL COMMUNICATION OVER FADING CHANNELS: Optimum coherent and non-coherent receiver in random amplitude, random phase channels- Performance of Rayleigh and Ricean channels, Performance of digital Modulation schemes such as BPSK, QPSK,FSK, DPSK, MSK etc. over wireless channels.

UNIT V
ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (OFDM): Carrier Synchronization, Timing synchronization, Multichannel and Multicarrier Systems.
TEXT BOOKS:

REFERENCES:
UNIT I
EIGEN ANALYSIS: Eigen Value Problem, Properties of eigen values and eigen vectors, Eigen Filters, eigen Value computations.
INTRODUCTION TO ADAPTIVE SYSTEMS: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner - Description, Weight Vectors, Desired Response Performance function, Gradient & Mean Square Error.

UNIT II
SEARCHING THE PERFORMANCE SURFACE – Methods & Ideas of Gradient Search methods, Gradient Searching Algorithm & its Solution, Stability & Rate of convergence - Learning Curves.

UNIT III
STEEPEST DESCENT ALGORITHMS: Gradient Search by Newton’s Method, Method of Steepest Descent, Comparison of Learning Curves.

UNIT IV
RLS ALGORITHM: Matrix Inversion lemma, Exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, convergence analysis of RLS Algorithm, Application of RLS algorithm on Adaptive Equalization

UNIT V
NON LINEAR ADAPTIVE FILTERING: Theoretical and Practical considerations of Blind Deconvolution, Buss Gang Algorithm for blind Equalization of real baseband Channels.
TEXT BOOKS:

REFERENCES:
UNIT I
INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

UNIT II
SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space
EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT III
RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

UNIT IV
INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor

UNIT V
SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design
DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes

TEXT BOOKS:
1. Computers as a component: principles of embedded computing system design-Wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:
1. Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2 Embedded system design - A unified hardware/software introduction - frank vahid, tony D.Givargis, John Willey, 2002
UNIT I
FUNDAMENTALS OF COMPUTER DESIGN: Elements of modern computers, Technology trends, cost-measuring and reporting performance quantitative principles of computer design.

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set-the role of compiler.

UNIT II
INSTRUCTION LEVEL PARALLELISM (ILP): overcoming data hazards, reducing branch costs, high performance instruction delivery, and hardware based speculation, limitation of ILP.


UNIT III
MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory. Synchronization, multi-threading.

UNIT IV
STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT V
INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster.

TEXTBOOKS:

REFERENCES:
2. Advanced Computer Architectures, Pearson Dezso Sima, Terence Fountain, Peter Kacsuk,
UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT III PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.
UNIT V
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

REFERENCES:
UNIT I
LOW POWER DESIGN, AN OVER VIEW: Introduction to low-voltage low power design, limitations, Silicon-on-Insulator.

UNIT II
LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.
DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT III
CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.
LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT IV
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT V
SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:
1. CMOS/BiCMOS ULSI low voltage, low power, Yeo Rofail/ Gohl(3 Authors), Pearson Education Asia 1st Indian reprint, 2002.

REFERENCES:
1. Simulation Rayleigh Fading Channel Using Either Clarke”s Model or Jake”s Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
3. Design and Simulation FIR Filter Using any Windowing Technique.
4. Design of IIR Filters from Analog Filters.
5. Performance Evaluation of QPSK System over Gaussian AWGN Channel.
7. Equalization of Multipath Channel using LMS or RLS Algorithms.
8. Performance Evaluation of RAKE Receiver over Slow Fading Channel.

NOTE: Use Mat lab
UNIT I
REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures.
THE 80286 MICRO PROCESSORS: Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNIT II
THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNIT III
THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)
INTRODUCTION TO MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Memory Management, Virtual Memory Concept of 80286 and other advanced Processors.

UNIT IV
ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

UNIT V
8096-MICROCONTROLLER: Introduction, Compare and contrast with 8051 microcontroller, Architecture and features, RAM structure, Register organization, Interrupts, Ports, Addressing modes and Instruction Set (brief treatment).

TEXTBOOKS:
2. Advanced Microprocessor and Peripherals, A.K. Ray and K.M. Bhurchandi, TMH.
REFERENCES:
UNIT I
IMAGE REPRESENTATION: Gray scale and color images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WT, Haar transform, KLT, DCT.

UNIT II
IMAGE ENHANCEMENT: Filters in spatial and frequency domains, histogram-based processing, and homomorphic filtering. Edge detection, non-parametric and model based approaches, LOG filters, localization problem.

UNIT III

IMAGE SEGMENTATION: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Hough transform, Region growing.

UNIT IV
IMAGE COMPRESSION: Compression models, Information theoretic perspective, Fundamental coding theorem.

LOSSLESS COMPRESSION: Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT V
VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation, Motion compensation, Video Filtering, Video Compression, Video coding standards.

TEXT BOOKS:

REFERENCES:
UNIT I
INTRODUCTION TO WIRELESS COMMUNICATION SYSTEMS: Evolution, Examples of Wireless Communication systems, Comparison, Second Generation Cellular Networks, WLL, Bluetooth and Personal Area Networks.

UNIT II

UNIT III
CELLULAR COMMUNICATION: Cellular Networks, Multiple Access: FDM/TDM/FDMA/TDMA, Spatial reuse, Co-channel interference Analysis, Hand over Analysis, Erlang Capacity Analysis, Spectral efficiency and Grade of Service- Improving capacity – Cell splitting and sectorization.

UNIT IV
SPREAD SPECTRUM AND CDMA: Motivation- Direct sequence spread spectrum- Frequency Hopping systems, Time Hopping., Anti-jamming- Pseudo Random (PN) sequence, Maximal length sequences, Gold sequences, Generation of PN sequences.

UNIT V
FADING CHANNEL CAPACITY: Capacity of Wireless Channels- Capacity of flat and frequency selective fading channels, Multiple Input Multiple output (MIMO) systems- Narrow band multiple antenna system model, Parallel Decomposition of MIMO Channels-Capacity of MIMO Channels.

TEXT BOOKS:
2. Modern Wireless Communications Simon Haykin and Michael Moher, Person Education.

REFERENCES:
UNIT I
SOURCE CODING-I: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for Discrete less sources, Source coding theorem, fixed length and variable length coding, properties of prefix codes.

UNIT II
LINEAR BLOCK CODES: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and correcting capability of Linear Block codes.

UNIT III
Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage Systems.

UNIT IV
CYCLIC CODES: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.
CONVOLUTIONAL CODES: encoding of Convolutional codes, Structural properties of Convolutional codes, state diagram, Tree diagram, Trellis Diagram, maximum, Likelihood decoding of Convolutional codes.

UNIT V
Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.
BCH CODES: Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2m), Basic properties of Falois Fields, Computation using Falois Field GF (2m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

TEXT BOOKS:
REFERENCES:
UNIT I
DETECTION THEORY: Binary decisions - Single observation - Maximum likelihood decision criterion, Neymann-Pearson criterion, Probability of error criterion, Bayes risk criterion, Min-max criterion, Robust detection, Receiver operating characteristics.

UNIT II
BINARY DECISIONS - MULTIPLE OBSERVATIONS: Vector observations, the general Gaussian Problem, Waveform Observation in Additive Gaussian Noise, The Integrating Optimum Receiver; Matched Filter Receiver.

UNIT III
ESTIMATION THEORY: Methods - Maximum likelihood estimation; Bayes cost method Bayes estimation criterion - Mean square error criterion; Uniform cost function; absolute value cost function; Linear minimum variance - Least squares method; Estimation in the presence of Gaussian noise - Linear observation; Non-linear estimation.

UNIT IV
STATE ESTIMATION: Prediction, Kalman filter.

UNIT V
SUFFICIENT STATISTICS AND STATISTICAL ESTIMATION OF PARAMETERS: Concept of sufficient statistics, Exponential families of Distributions, Exponential families and Maximum likelihood estimation, uniformly minimum variance unbiased estimation.

TEXT BOOKS:

REFERENCES:
UNIT I
NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture.

UNIT II
ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT III
ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections. QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT IV
REARRANGEABLE NETWORKS: Re-arrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT V

TEXT BOOKS:
1. ISDN & B-ISDN with Frame Relay, William Stallings, PHI.

REFERENCES:
2. ATM Networks, Rainer Handel, Manfred N.Huber, Stefan Schroder, Pearson Edu, 2002
3. High Speed Networks and Internets, William Stallings, Pearson edu., 2002
UNIT I
OPTICAL FIBER COMPONENTS: couplers, Isolators and Circulators, Multiplexers, Bragg grating, Fabry-perot Filters, Mach zender interferometers, Arrayed waveguide grating, tunable filters, hi-channel count multiplexer architectures, optical amplifiers, direct and external modulation transmitters, pump sources for amplifiers, optical switching and wave length converters.

UNIT II

UNIT III

UNIT IV

UNIT V

TEXT BOOKS:
REFERENCE BOOKS
UNIT I
REVIEW OF INFORMATION THEORY: The discrete memory-less information source, Kraft inequality; optimal codes Source coding theorem. Compression Techniques, Lossless and Lossy Compression, Mathematical Preliminaries for Lossless Compression, Huffman Coding, Optimality of Huffman codes, Extended Huffman Coding, Adaptive Huffman Coding, Arithmetic Coding, Adaptive Arithmetic coding, Run Length Coding.

UNIT II
QUANTIZATION: Uniform & Non-uniform, optimal and adaptive quantization, vector quantization and structures for VQ, Optimality conditions for VQ, Predictive Coding, Differential Encoding Schemes

UNIT III
MATHEMATICAL PRELIMINARIES FOR LOSSY CODING: Rate distortion theory: Rate distortion function R(D),Properties of R(D); Calculation of R(D) for the binary source and the Gaussian source, Rate distortion theorem, Converse of the Rate distortion theorem.

UNIT IV
MATHEMATICAL PRELIMINARIES FOR TRANSFORMS: Karhunen Loeve Transform, Discrete Cosine and Sine Transforms, Discrete Walsh Hadamard Transform, Lapped transforms- Transform coding, Sub-band coding, Wavelet Based Compression, Analysis/Synthesis Schemes.

UNIT V
IMAGE COMPRESSION STANDARDS: Binary Image Compression Standards, Continuous Tone Still Image Compression Standards, Video Compression Standards.

TEXT BOOKS:

REFERENCES:
SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(16EC3815) DIGITAL SYSTEM DESIGN LAB

M.Tech I Year -II SEM (DECS) L  P  C
0  4  2

CYCLE 1:

1. Simulation and Verification of Logic Gates.
2. Design and Simulation of Half adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder and Full Adder.
3. Simulation and Verification of Decoder, MUXs, Encoder using all Modeling Styles.
5. Design and Simulation of Counters-Ring Counter, Johnson Counter, and Up-Down Counter, Ripple Counter.
7. Design of Sequence Detector (Finite State Machine-Mealy and Moore Machines).
8. 4-Bit Multiplier, Divider. (for 4-Bit Operand)
9. Design ALU to Perform –ADD, SUB, AND-OR, 1’s and 2’s COMPLIMENT, Multiplication, Division.

CYCLE 2: After completing cycle 1,

Digital Circuit Description Using Verilog / VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
4. Place and Router Techniques for FPGA’s like Xilinx, Altera, Cypress, etc.,