SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : (13A04507) **Course & Branch**: B.Tech - CSE

Year & Sem: III-B.Tech & I-Sem **Regulation:** R13

UNIT –I

Microprocessors-Evolution and Introduction

1. Draw and explain the architecture of 8085. [CO1]**[LI]10M**
2. Explain all addressing modes of 8085 with related examples. [CO2]**[L4]10M**
3. (a) Compare the features of 8086 and 8085 processor. [CO1]**[L4]03M**
   (b) Explain how pipelining is achieved in 8086. [CO1]**[L1]02M**
   (c) Define the function of following pins in 8086. [CO1]**[LI]05M**
   (i)ALE (ii) INTR (iii) HOLD (iv)$\overline{TEST}$ (v) DT/$\overline{R}$
4. Explain with neat diagram how 8086 access a byte or word from even and odd memory banks. [CO1]**[LI]10M**
5. Draw and explain the architecture of 8086. [CO1]**[LI]10M**
6. (a)Explain the concept of segmented memory. What are its advantages? [CO1]**[LI]05M**
   (b)Write the differences between procedure and macro with an example. [CO2]**[LI]05M**
7. (a)Briefly explain the register organization of 8085. [CO1]**[LI]05M**
   (b) Define interrupt & Types of interrupts in 8085. [CO1]**[LI]05M**
8. Related to 8086 define the functions of pins used in [CO1]**[LI]2*5M**
   (a) Minimum mode
   (b) Maximum mode.
9. Explain in detail the register organization of 8086. [CO1]**[LI]10M**
10. a) Differentiate microprocessor and microcontroller. [CO1]**[LI]2M**
    b) Compare the microprocessor 8086 with 8085 [CO1]**[L3]2M**
    c) What is the difference between PC and instruction pointer (IP)? [CO1]**[LI]2M**
    d) Define System BUS and their types? [CO1]**[LI]2M**
    e) What is the function of DAA, XCHG and AAD instructions in 8086? [CO2]**[LI]2M**

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UNIT –II

Addressing modes, Instruction set and Programming of 8086

1. Describe the addressing modes of 8086 with suitable examples. [CO2]**[L4]10M**
2. Write an ALP program to sort the given numbers 08, 02, 07,03,06,04 and 05 in ascending order with flow chart. [CO2]**[L4]10M**
3. (a)explain the following instructions [CO2]**[LI]5M**
   (i)AAM (ii) DAA (iii) CBW (iv) LAHF/SAHF (v) LDS
   (b) Explain the addressing modes of 8086 with examples [CO2]**[L4]5M**
   (i) Register addressing mode
   (ii) Indirect addressing mode.
   (iii) Relative index addressing mode
4. With the help of examples define [CO2]**[LI]2*5M**
   (a) Logical instructions
   (b) Flag manipulation instructions
5. Explain (a) shift and rotate instructions [CO2]**[LI]2*5M**
   (b) Arithmetic instructions
6. (a)what is the function of DAA instruction in 8086. [CO2]**[LI]3M**
   (b) What is the function of D and I flags in 8086? [CO1]**[LI]2M**
   (c) Define PUSH and POP instructions in 8086? [CO2]**[LI]5M**
7. Write an ALP to add the multi-byte data F2354687H with C545689FH and store the result from the address 1000H: 2000H in the memory, with the lower order byte of result stored first. [CO2]**[LI]10M**
8. (a)Explain the purpose of following directives. [CO2]**[LI]2*5M**
   (i)ORG (ii) EQU (iii) ASSUME (iv) MODEL (v) DW
   (b)Describe the following instructions of 8086 with examples.
   (i)STOS. (ii)TEST. (iii)ROL. (iv)CMC

9. (a)Define modular programming. List its features, advantages and disadvantages. [CO1]**[LI]5M**

   (b) Compare procedure with macro. [CO1] **[LI]05M**

10. (a)Define addressing mode? And their types in 8086 microprocessor. [CO1] **[LI]2M**

    (b) How many memory locations can be addressed by a microprocessor with 14 address lines and draw its address mapping. [CO2] **[LI]02M**

    (c) List the available in branching instruction types in 8086 instruction set. [CO2] **[LI]2M**

    (d) What is the function of BHE' and ALE signals in the 8086? [CO1] **[LI]2M**

    (e) find the memory address from where the data can be accessed in the instruction, Mov BX, [SI-110H], if segment address is 3000H and EA Is 1000H. [CO2] **[LI]2M**

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UNIT –III

8086 Interrupts, Memory and I/O Interfacing

1. Draw and explain interrupt vector table of 8086. [CO3]**[LI]10M**
2. Interface two 8K X 8EPROMS (2764) with the 8086 using logic gates such that the memory address ranges assigned to them are FC000H – FFFFFH? [CO3]**[[L6]10M**
3. Interface 16-bit output port to 8086.The output port should be mapped in memory with address 40000H. [CO3]**[[L6]10M**
4. Interface two 8K X 8EPROMS (2764) with the 8086 using an address decoder made up of the 74138 IC and logic gates such that the memory address ranges assigned to them are FC000H – FFFFFH? [CO3]**[[L6]10M**
5. Interface four 8K X 8 RAM chips (6264) with the 8086, to assign the address range 80000H-87FFFH using two 74138 ICs. [CO3]**[[L6]10M**
6. Interface two 8K x 8 RAM chips (6264) with the 8086 using logic gates such that the memory address ranges assigned to them are 00000H – 03FFFH? [CO3]**[[L6]10M**
7. (a) Define I/O interfacing. [CO3]**[[LI]3M**
   (b) Define I/O instructions in 8086? [CO3]**[[LI]3M**
   (c) Explain I/O mapped and memory-mapped I/O. [CO3]**[[LI]5M**
8. Describe how to Interface a CRT terminal with 8086. [CO3]**[[L3]10M**
9. Define all the BIOS interrupts. [CO3]**[[LI]10M**
10. (a) Difference between Memory mapped IO and IO mapped IO. [CO3]**[[LI]2M**
    (b) Write the major steps involved in interrupt service. [CO3]**[[LI]2M**
    (c) Describe the function of AEN and DT/R'. [CO3]**[[LI]2M**
    (d) How to enable and disable interrupts in 8086? [CO3]**[[LI]2M**
    (e) What is effective address? How it can be specified in instruction. [CO3]**[[L4]2M**

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UNIT –IV

Features and Interfacing of Programmable devices for 8086 System

1. Describe sequence of operations during data transfer between CPU and memory using 8237 DMA controller. [CO4]**[[LI]10M**
2. Explain mode-0 mode-1 and mode-2 of 8253 timer with neat timing diagrams. [CO4]**[[LI]10M**
3. Explain the internal architecture of 8237 with its features. [CO4]**[[LI]10M**
4. Explain the internal architecture of 8251 with its features. [CO4]**[[LI]10M**
5. (a) With neat sketch how an 8255 is interfaced with 8086. [CO4]**[[L3]5M**
   (b) Explain how 7-segment display can be interfaced with 8086. [CO4]**[[L3]5M**
6. Explain the internal architecture of 8255 with its features. [CO4]**[[LI]10M**
7. With the help of diagrams describe
   (a) Interfacing ADC chip with 8086. [CO4]**[[L3] 5M**
   (b) Interfacing push button switches and LEDs with 8086. [CO4]**[[L3] 5M**
8. (a)Draw and explain the internal architecture of 8259? [CO4]**[[LI]5M**
   (b) Show the format of ICW-1, ICW-2. [CO4]**[[LI] 5M**
9. (a) List the hand shaking signals required for MODEM interface using 8251. [CO4]**[[LI]4M**
   (b) Write control word to set bit-4 of port C of 8255. [CO4]**[[L4]4M**
   (c) What is the function of In-service register in 8086? [CO4]**[[LI]2M**
10. (a)Discuss about mode-3 operation in 8053 timer. [CO4]**[[LI]2M**
    (b)Define the role of address lines A0 & A1 in 8255? [CO4]**[[L4]2M**
    (c)List any three features of 8253. [CO4]**[[LI] 2M**
    (d)Define the command register in 8237. [CO4]**[[LI]2M**
    (e)Discuss about mode-2 operation in 8053 timer. [CO4]**[[LI]2M**

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QUESTION BANK (DESCRIPTIVE)

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Year & Sem: III-B.Tech & I-Sem **Regulation:** R13

UNIT –V

Introduction to 8051 Microcontrollers

1. Draw and explain internal structure of port 1 of 8051 [CO5]**[[LI]10M**
2. Draw and explain the architecture of 8051. [CO5]**[[LI]10M**
3. With the help of diagrams. Explain
   (a) Interfacing of 7-segment display with 8051. [CO6] **[L3]5M**
   (b) Interfacing push button switches and LEDs with 8051. [CO6] **[L3]5M**
4. Explain in detail about 8051 serial ports? [CO5] **[LI]10M**
5. Explain in detail the different operating modes of timer in 8051. [CO5] **[LI]10M**
6. Define the following:
   (a) Interrupt sources and interrupt vector address**.** [CO5] **[LI]4M**
   (b) Enabling and disabling interrupts. [CO5] **[L3]3M**
   (c) Interrupt priorities and polling sequence. [CO5] **[LI]3M**
7. Briefly discuss about the bit patterns of
   (a)TMOD register. [CO5] **[LI]5M**
   (b) TCON register. [CO5] **[LI]5M**
8. (a)Draw and explain the structure of port-1 port-2 of 8051. [CO5] **[LI]5M**
   (b) Show the bit patterns of TMOD special function register. [CO5] **[LI] 5M**
9. Sketch and explain the interfacing of
   (a) External program memory to 8051. [CO6] **[L4]5M**
   (b) External data memory to 8051. [CO6] **[L4]5M**
10. (a) State extra hardware features of 8051 as compared to microprocessor. [CO5] **[LI]2M**
    (b)List the important features of 8051. [CO5] **[LI]2M**
    (c) Explain the difference in stack operation with regard to 8086 and 8051. [CO5] **[LI]2M**
    (d) Write difference between MOVX and MOVC. [CO5] **[LI]2M**
    (e) Explain TCON and TMOD function registers of 8051. [CO5] **[LI]2M**

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Year & Sem: III-B.Tech & I-Sem **Regulation:** R13

UNIT –I

Microprocessors-Evolution and Introduction

1. Supply voltage 'VCC' of 8085 µp is……volts [ ]
   A) 2 B) 3 C) 4 D) 5
2. The address bus flow in _____ [ ]
   A) Bidirectional B) unidirectional
   C) Multidirectional D) Circular
3. The first part of an instruction which specifies the task to be performed by the computer is called _____ [ ]
   A) opcode B)operand C)instruction cycle D)fetch cycle
4. Number of T-states required to execute the instruction MOV L,H is [ ]
   A) 10 B) 4 C) 7 D) 13
5. 8085 µp has …… no. of instructions. [ ]
   A) 246 B) 256 C) 266 D) 286
6. In 8085µp the no. of software interrupts? [ ]
   A) 5 B) 7 C) 8 D) 9
7. Status register is also called as _____ [ ]
   A) Accumulator B) Stack C) Counter D) flags
8. The address / data bus in 8085 is _____ [ ]
   A) Multiplexed B) de-multiplexed C) decoded D) loaded
9. No. of input pins in 8085 µp… [ ]
   A) 21 B) 27 C) 29 D) 23
10. Can ROM be used as stack? [ ]
    A) Yes B) No C) sometimes yes, sometimes no
11. PUSH and POP instructions are related to .. [ ]
    A) Program counter B) queue C) stack D) DMA controller
12. The status of S0 and S1 pins for memory write is. [ ]

A)0, 0 B)0,1 C)1,0 D)1,1

13. No. of output pins in 8085 µp… [ ]

A)21 B)27 C)29 D)23

14. In 8086, Example for Non Vectored interrupts are.. [ ]

A) Trap B) RST6.5 C) INTR D) All the above

15. Address line for RST 3 is [ ]

A) 0020H B) 0028H C) 0018H D) 0038H

16. Itanium processor of Intel is a [ ]

A) 32 bit microprocessor. B)64 bit microprocessor.

C)128 bit microprocessor. D)256 bit microprocessor.

17. The second part of the instruction is the data to be operated on, and it is called [ ]

A) opcode B)operand

C) Instruction cycle D) Mnemonic

18. What is meant by Maskable interrupts? [ ]

A) An interrupt which can never be turned off.

B) An interrupt that can be turned off by the programmer. C) None

19. The status of S0 and S1 pins for memory fetch is. [ ]

A)0, 0 B)0, 1 C)1,0 D)1,1

20. TRAP Triggering interrupts is also called as.. [ ]

A) INTR B) RST 6.5 C) RST7.5 D) RST4.5

21. Which of the following is level triggered interrupt in 8085? [ ]

A) RST6.5 B) RST 5.5 C) INTR D) all the above.

22. Which of the following is the fastest memory element? [ ]

A) Cache B) primary C) secondary D) processor

23. Ready pin of a microprocessor is used [ ]

A) To indicate that the microprocessor is ready to receive inputs.

B) To indicate that the microprocessor is ready to receive outputs.

C) To introduce wait states.

D) To provide direct memory access.

24. The no. of address lines required to address a memory of size 32 K is [ ]

A) 15 lines B) 16 lines C) 18 lines D) 14 lines

25. The stack is a specialized temporary access memory during ……instructions [ ]

A)random, store, load B)random, push, load

26. C)sequential, store, pop D)sequential, push, pop

27. 8085 has …… software restarts and ….. hardware restarts [ ]

A)10, 5 B)8,5 C)7,5 D)6,6

28. TRAP is …..Whereas RST 7.5, RST 6.5, RST 5.5 is…. [ ]

A)maskable, non maskable B)maskable, maskable

C)non - maskable, non – maskable D)non - maskable, maskable

29. Parity flag will be set, when the result has an ……. [ ]

A) Even no.of ones B) odd no.of ones C) both D) none

30. Pseudo instructions are basically [ ]

A) False instructions. B) Instructions that are ignored by the microprocessor.

C) Assembler directives. D) Instructions that are treated like comments.

31. SP always holds the address of the …… [ ]

A) Bottom of the stack B) top of the stack C) middle of the stack d) all

32. Auxiliary carry flag is used during …… [ ]

A) hex-decimal addition B) BCD addition C)binary addition d)all of the above

33. AC flag is set when there is a carry from ……. [ ]

A) Lower nibble to higher nibble

B) Higher nibble to lower nibble C) any D) none

34. The interrupt vector address for TRAP is [ ]

A) 0000H B) 0024H C) 0018H D) 002CH

35. Which of following is both level and edge sensitive? [ ]

A) RST 7.5 B) RST 5.5 C) TRAP D) INTR

36. The width of address bus and data bus in 8085 are respectively …. [ ]

A) 16, 8 B) 8, 16 C) 8, 8 D) 16, 16

37. _____ is flip-flop which indicates some condition which arises after the execution of an arithmetic or logic instruction. [ ]

A) Accumulator B) Temporary register C) Status flag D) program counter

38. …….are used for DMA operation? [ ]

A) HOLD & HLDA B) ALE

C) READY D) SID and SOD

39. The……µp is first invented in….. Using…..Technology. [ ]

A)4001,1971,PMOS B)4004,1972,NMOS

C)4040,1971,PMOS D)4004,1971,PMOS

40. Operating frequency of 8085 µp is…MHz [ ]

A) 2 B) 3 C) 4 D) 5

41. Which interrupt has the highest priority? [ ]

A) INTR B) TRAP C) RST6.5 D) RST 7.5.

42. The first µp was invented by [ ]

A) Ted Hoff B) Stanley mozar C) M. shima D) all

43. MATCH THE FOLLOWING [ ]

GROUP A	GROUP-B
I-Generation	1. 1981-1995
II-Generation	2. 1978-1980
III-Generation	3. 8-bit µp
IV-Generation	4. 16-bit µp

A)4,3,2,1 B)3,4,2,1 C)4,1,3,2 D)3,4,1,2

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UNIT –II

Addressing modes, Instruction set and Programming of 8086

1. In 8086 microprocessor one of the following statements is not true. [ ]
   A) Coprocessor is interfaced in MAX mode B) Coprocessor is interfaced in MIN mode
   C)I/O can be interfaced in MAX / MIN mode D) supports pipelining.
2. Direction flag is used with [ ]
   A) String instructions. B) Stack instructions.
   C) Arithmetic instructions. D) Branch instructions.
3. Ready pin of a microprocessor is used [ ]
   A) To indicate that the microprocessor is ready to receive inputs.
   B) To indicate that the microprocessor is ready to receive outputs.
   C) To introduce wait states.
   D) To provide direct memory access.
4. The index register are used to hold _____ [ ]
   A) Memory register B. offset address C. segment memory D. offset memory
5. Which of the following is the fastest memory element? [ ]
   A) Cache B) primary C) secondary D) processor
6. What is meant by Maskable interrupts? [ ]
   A) An interrupt which can never be turned off.
   B) An interrupt that can be turned off by the programmer. C) None
7. The register AX is formed by grouping _____ [ ]
   A) AH & AL B) BH & BL
   C.)CH & CL D) DH & DL
8. The work of EU is _____ [ ]
   A) Encoding B) decoding C) processing D) calculations

9. IMUL source is a signed _____ [ ]

A) Multiplication B) addition C) subtraction D) division

10. The IP is _____ bits in length [ ]

` A)8 bits B) 4 bits C) 16 bits D) 32 bits

11. Example of Immediate addressing mode… [ ]

A) MOV AX, 2000H B) MOV AX, BX

C) MOV AX, [2000H] D) none

12. BHE of 8086 microprocessor signal is used to interface the [ ]

A) Even bank memory B) Odd bank memory

C)I/O D) DMA

13. In 8086 the overflow flag is set when [ ]

A) The sum is more than 16 bits

B) Signed numbers go out of their range after an arithmetic operation

C) Both D) none

14. Example of register addressing mode… [ ]

A) MOV AX, 2000H B) MOV AX, BX

C) MOV AX, [2000H] D) none

15. In 8086, Example for Non Vectored interrupts are.. [ ]

A) Trap B) RST6.5 C) INTR D) All the above

16. The stack is a specialized temporary access memory during &..instructions [ ]

A) random, store, load B)random, push, load

C) Sequential, store, pop D) sequential, push, pop

17. When we use RRC instruction once in 8085, the number is [ ]

A) Multiplied by 2 B) divided by 2
C) Multiplied by 4 D) divided by 4

18. What will be the contents of r AL after the following has been executed [ ]

MOV BL, 8C

MOV AL, 7E

ADD AL, BL

(A) 0A and carry flag is set (B) 0A and carry flag is reset

(C) 6A and carry flag is set (D) 6A and carry flag is reset

19. 8086 processor is an ……. [ ]

A) Sequential Device B) pipelined architecture C) both D) none

20. The size of instruction queue in 8086 is…….. [ ]

A) 4-byte long B) 5-byte long

C) 6-byte long D) 2-byte long

21. The total number of registers in 8086 is…….. [ ]

A) 13 B) 10 C) 12 D) 14

22. The sizes of all registers in 8086 are ….. [ ]

A) 32-bit B) 4-bit C) 8-bit D) 16-bit

23. In 8086 processor, the EU and BIU operate … [ ]

A) Serially B) in-phase C) Asynchronous D) Synchronous

24. In 16-bit to 8-bit division operation, the quotient and remainder store at… [ ]

A) AH-AL B) AL-AH C) AX-DX D) DX-AX

25. In 32-bit to 16-bit division operation, the quotient and remainder store at… [ ]

A) AH-AL B) AL-AH C) AX-DX D) DX-AX

26. Instructions IN and OUT are related to …. [ ]

A) AX B) BX C) CX D) all

27. The basic operation done in the instruction TEST is….. [ ]

A) OR B) AND C) XOR D) SUB

28. The basic operation done in the instruction CMP is….. [ ]

A) OR B) AND C) XOR D) SUB

29. Decrement CX is happened automatically in ……. [ ]

A) LOOP B) REP C) TEST D) both A and B

30. The instruction PUSH BX indicates… [ ]

A) Decrement SP by 2 B) Decrement SP by 2

C) Decrement SP by 1 D) Decrement SP by 1

31. The instruction NEG indicates… [ ]

A) 1s complement B) 2s complement

C) No complement D) none

32. The instruction **MOV [BX+SI], BP** belongs to …..Addressing mode [ ]

A) Base B) base-index

C) base-index with displacement D) index

33. The instruction **ADD AX,[1234H]** belongs to …..Addressing mode [ ]

A) Base B) base-index

C) Register D) direct

34. The instruction **ADD AX, [SI];** belongs to …..Addressing mode [ ]

A) Base B) base-index

C) Index D) register in-direct

35. The instruction **MOV AX,[BP+1]**belongs to …..Addressing mode [ ]

A) Base-relative B) base-index

C) Index D) direct

36. In 8086 IP will act as… [ ]

A) Program counter B) stack pointer

C) Base pointer D) data pointer

37. The index register are used to hold _____ [ ]

A) Memory register B) offset address C) segment memory D) offset memory

38. The segment register are used to hold _____ [ ]

A) Base address B) offset address C) segment memory D) offset memory

39. Status register is also called as _____ [ ]

A) Accumulator B) Stack C) Counter D) flags

40. The 8086 fetches instruction one after another form _____ of memory [ ]

A) Code segment B) IP C) ES D) SS

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UNIT –III

8086 Interrupts, Memory and I/O Interfacing

1. In 8086 microprocessor one of the following statements is not true. [ ]
   A) Coprocessor is interfaced in MAX mode
   B) Coprocessor is interfaced in MIN mode
   C) I/O can be interfaced in MAX / MIN mode
   D) supports pipelining.
2. Interrupt controls the serial communication ports attached to the computer [ ]
   A) INT 01H B) INT 31H C) INT 14H D) INT 13H
3. ……. Instruction is used to be executed at the end of the interrupt service routine to return to the interrupted program [ ]
   A) RET B) BACK C) IRET D) BREAK
4. There are ….. interrupts types in 8086 microprocessor [ ]
   A) 255 B) 156 C) 254 D) 256
5. Which is the type of interrupt that takes value between 00H to FFH : [ ]
   A) NMI B) Software interrupt
   C) Hardware interrupt D) Trap
6. If an interrupt has been requested, 8086 processes it by [ ]
   A) Pushing the content of IP onto stack by decrementing SP by 2
   B) Pushing the content of CS onto stack by incrementing SP by 2
   C) Sets TF in the flag register D) None
7. In 8086, first 1KB of memory is set aside as…… for storing interrupts [ ]
   A) TVI B) IVT C) CS: IP D) DS
8. What type of interrupt is generated when DIV or IDIV operation is too large to fit in the result
   A) TYPE 0 B) TYPE 1 C) TYPE 2 d) TYPE 3

9. ……. Interrupt is also used to sense the hazardous situations such as fire, smoke and unsafe pressure or temperature limits in an industrial environment. [ ]

A) TRAP B) NMI C) single step D) RESET

10. . …… is used to insert a breakpoint in a program for debugging [ ]

A) INT 21H B) INT 05H C) INT 03H D) INT 08H

11. ……. Is the lowest priority interrupt in 8086 microprocessor [ ]

A) NMI B) INTR C) single step D) INT 0

12. is the boot firmware which is designed to be the first program run by PC when powered on [ ]

A)BIOS B)DOS C)COM D)none

13. ……. Is the video services interrupt directly controls the video display in a system [ ]

A) INT 01H B) INT 02H C) INT 03H D) INT 04H

14. . ….. is used to determine the type of equipment installed in the system [ ]

A) INT 01H B) INT 11H C) INT 12H D) INT 15H

15. ……. is used to control various I/O devices interfaced with the computer [ ]

A) INT 11H b) INT 01H C) INT 15H D) INT 14H

16. ……. Is used to control the keyboard in a system [ ]

A) INT 01H B) INT 05H C) INT 16H D) INT 13H

17. . These are the functions provided by the OS such as library functions, to handle I/O operations [ ]

A) Direct access B) HLL C) DOS services D) BIOS services

18. The most common I/O data transfer technique used in the Intel microprocessor based system is I/O mapped I/O is called… [ ]

A) Isolated I/O scheme B) Combined I/O scheme

C) Grouped I/O scheme D) none

19. 74LS244 is ….. [ ]

A) Encoder B) Decoder C) Multiplexer D) Buffer

20. ……. Is an active low signal that activates when the printer is in offline state or paper end state [ ]

A) INIT B) SLCTIN C) SLCT D) ERROR

21. The CRT terminal uses the ….. for communication with the processor [ ]

A) RS-232 B) UART C) TTL D) USART

22. The interrupt service…. Is used to warm reboot [ ]

A) 05H B) 12H C) 19H D) 1AH

23. Before issuing the command INT 21H the sub-function code has to be loaded Into…. Register [ ]

A) AL B) AX C) AH D) CX

24. . …. is the function provided by INT 15H to set watchdog timer [ ]

A) C4H B) C2H C) C3H D) C4H

25. The…. provide access to the parallel printer port called LPTI in most systems [ ]

A) INT 12H B) INT 11H C) INT 17H D) INT 15H

26. TYPE 03H is also called as….. interrupt [ ]

A) one-byte INT B) NMI C) Divide by zero D) single step

27. The BIOS program is always located in a special reserved area from the address [ ]

A) F0000H to FFFFFH B) 00000H to FFFFFH

C) 11111H to FFFFFH D) none

28. …… is used to print all the printable characters present on the screen either in Text or graphics mode [ ]

A) INT 01H B) INT 02H C) INT 03H D) INT 05H

29. …….. is necessary to initialize the printer port, write characters, or read the Status of the printer [ ]

A) INT 17H B) INT 01H C) INT 05H D) INT 07H

30. instruction is used to read the data from an input device to AL or AX in the 8086 [ ]

A) OUT B) IN C) BUF D) none

31. Signal is used to enable the upper bank of the memory and odd I/O bank in 8086 [ ]

A) ALE B) BHE C) STROBE D) IOR

32. IC 8251 is… [ ]

A) Encoder B) Decoder C) Multiplexer D) USART

33. The difference between the data and the command is achieved by means of …. Codes [ ]

A) Escape B) error C) debug D) none

34. BIOS functions has … types of routines [ ]

A) One B) two C) three D) four

35. INT 21H is used to…operations [ ]

A) Memory read B) memory write C) I/O D) decode

36. IV is a....bit entry into IVT which contains a 16-bit offset part and 16-bit segment part.[ ]

A) 2 B) 4 C) 5 D) 6

37. .. ……..is a maskable hardware interrupt in 8086 that can be enabled/disabled using the flag [ ]

A) INTR B) TRAP C) RESET D) none

38. KBD_INT, the name given to the default BIOS keyboard ….handler, reads the scan code from 60H [ ]

A) INT 11H B) INT21H C) INT 31H D) INT 41H

39. VGA stands for [ ]

A) Visual Graphics Array B) Visual Graph Array

C) Video Graphics Array D) Visualized Graphics Array

40. By calling the function code 0BH of video services,…is done [ ]

A) Get cursor position and shape B) set border color

C) Clear screen up D) get light pen position

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QUESTION BANK (OBJECTIVE)

Subject with Code : (13A04507) **Course & Branch**: B.Tech - CSE

Year & Sem: III-B.Tech & I-Sem **Regulation:** R13

UNIT –IV

Features and Interfacing of Programmable devices for 8086 System

1. IC 8255 is a ….. [ ]
   A) PPI B) PIC C) DMA D) USART
2. IC 8255 has three …..bit TTL compatible registers or ports [ ]
   A) 1 B) 2 C) 4 D) 8
3. Port C of IC 8255 is selected when A1 and A0 are [ ]
   A) 0,0 B)0,1 C)1,0 D)1,1
4. Group A of IC 8255 comprises of [ ]
   A) Port A and PCU B) Port B and PCL
   C) Port B and PCU D) Port A and PCL
5. The Pin number of RESET signal in IC 8255 is [ ]
   A) 36 B) 35 C) 32 D) 31
6. In IC 8255, BSR mode is operated when D7 bit in the control word is [ ]
   A) 0 B) 1 C) 2 D) none
7. In Mode 2 of IC 8255, Port C is operated for…. [ ]
   A) Programming B) bidirectional C) handshaking D) latching
8. What type of mode in IC 8255 is used for transferring I/O data to or from a specified port in conjunction with strobes. [ ]
   A) Mode 1 B) Mode 2 C) Mode 3 D) BSR
9. In mode 2 of IC 8255, data is transmitted and received via …. [ ]
   A) Port A B) Port B C) Port C D) Port D
10. The simplest hardware solution to suppress the bouncing is: [ ]
    A) LC circuit B) RC circuit C) RLC circuit D) none

11. In common Anode display, to illuminate a segment, the segment must be Connected to… [ ]

A) Logic 0 B) Logic 1 C) Supply D) none

12. In common Cathode display, to illuminate a segment, the segment must be Connected to… [ ]

A) Logic 0 B) Logic 1 C) Supply D) none

13. IC 7447 is a… [ ]

A) Encoder B) Decoder C) Multiplexer D) Latch

14. The smallest change in the input voltage that can be sensed or detected at the output of an ADC is called: [ ]

A) Monotonicity B) Resolution C) Accuracy D) Bandwidth

15. The analog to Digital conversion can be started by using active high control signal…….. [ ]

A) SC B) EOC C) OE D) ALE

16. The LSB of ….. is used to check the end of conversion signal [ ]

A) Port A B) Port B C) Port C D) Port D

17. Example of DAC … [ ]

A) Successive approximation B) Flash

C) Dual slope D)R-2R ladder

18. ……is a measure of how straight the output is changed from minimum value to the maximum value [ ]

A) Resolution B) Linearity C) Accuracy D) Monotonicity

19. The DAC…. Is a common digital to Analog converter chip that can be easily interfaced to the 8086 through 8255 [ ]

A)0800 B)0816 C)0804 D)0808

20. The…. is defined as the time taken for the output to settle within the pre-specified band after the input digital value is achieved [ ]

A) Flying time B) Storage time

C) Settling time D) Transition time

21. IC 8253 is a….. [ ]

A) PPI B) PIC C) Timer D) ROM

22. The maximum operating frequency of IC 8253 is…. [ ]

A) 8.5MHz B) 6.2MHz C) 2.6MHz D) 3.2MHz

23. IC 8253 consists of ……16-bit timers [ ]

A) 2 B) 3 C) 4 D) 5

24. 11th pin of IC 8253 is… [ ]

A) Gate 0 B) Gate 1 C) CLK2 D) CLK1

25. 25. The number of operating modes of IC 8253 …. [ ]

A) 2 B) 4 C) 6 D) 8

26. The operation of……mode is similar to that of a mono-stable multi-vibrator in IC 8253 [ ]

A) 0 B) 1 C) 2 D) 3

27. Mode…..of IC 8253 is called as Software-triggered Strobe [ ]

A)1 B)2 C)3 D)4

28. Mode 3 of IC 8253 is called as…. [ ]

A) Rate generator B) Square wave generator

C) Interrupt on Terminal count D) Hardware triggered one shot

29. Which mode of IC 8253 acts as Divide- by- N-counter [ ]

A) 0 B) 1 C) 2 D) 3

30. In ……..transmission, the communication can take place in either direction between systems but only in one direction at a time [ ]

A) Simplex B) half duplex C) full duplex D) none

31. ….. is the rate at which serial data is being transferred [ ]

A) Synchronous transmission B) Baud rate

C) Asynchronous transmission D) none

32. IC 8259 is a… [ ]

A) PPI B) PIC C) USART D) Decoder

33. One of the registers of IC 8259 is… [ ]

A) ISR B) W C) HL D) SP

34. The …. of IC 8259 maintains a list of the current interrupts that are pending Acknowledgement [ ]

A) IRR B) ISR C) IMR D) IP

35. Which word is used to specify the priorities of interrupts and issue of end of interrupt commands [ ]

A) OCW1 B) OCW2 C) ICW2 D) ICW3

36. The ….. is a method of data transfer between memory and I/O peripherals without the intervention of the microprocessor [ ]

A) USART B) Serial I/O C) DMA D) pipelining

37. IC 8237 is a… [ ]

A) USART B) DMA C) Serial controller D) PIC

38. IC 8237 contains….no. of DMA channels [ ]

A) 1 B) 2 C) 3 D) 4

39. . …….register of IC 8237 determines the no.of transfers to be performed [ ]

A) Command address B) current word count

C) Command D) base address

40. In the ….mode of IC 8237, the device continues making transfers until a TC or external EOP is encountered [ ]

A) Block transfer B) cascade C) demand transfer D) single transfer

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QUESTION BANK (OBJECTIVE)

Subject with Code : (13A04507) **Course & Branch**: B.Tech - CSE

Year & Sem: III-B.Tech & I-Sem **Regulation:** R13

UNIT – V
Introduction to 8051 Microcontrollers

1. …….are the processor chips that generally have memory, input ports and Output ports within the chip itself [ ]
   A) Microprocessor B) Microcontroller C) NOC D) none
2. Intel 8051 contains …..ports and ….16-bit timers [ ]
   A)4,2 B)2,4 C)1,3 D)3,1
3. When 8051 is reset, the stack pointer is by default set to… [ ]
   A)00H B)02H C)05H D)07H
4. Register bank can be selected by…..bits in the flag register [ ]
   A)P B)OV C)F0 D)RS0 and RS1
5. The address range of bank3 in 8051 [ ]
   A)00H-07H B)08H-0Fh C)10H-17H D)18H-1Fh
6. The microcontroller enters the idle mode whenever… [ ]
   A) PCON.0 bit is 0 B) PCON.0 bit is 1
   C)SCON.0 bit is 0 D)SCON.0 bit is 1
7. Power down mode is initiated by making… [ ]
   A) PCON.0 bit is 0 B) PCON.0 bit is 1
   C)PCON.1 bit is 0 D)PCON.1 bit is 1
8. The stack pointer in 8051 is an 8-bit register within the SFR with address… [ ]
   A)80H B)81H C)82H D)84H
9. MOVC A, @A+DPTR is an example of …. Addressing mode [ ]
   A) Immediate B) Register direct C) Memory indirect D) Indexed
10. The mnemonics of Call subroutine at PC:addr is [ ]
    A)LCALL addr B)ACALL 11-bit addr
    C)LJMP addr D)AJMP 11-bit addr

11. . …..port of 8051 is used exclusively for input and output operations [ ]

A)1 B)2 C)3 D)4

12. Port3.1 of 8051 is used as [ ]

A) RXD B) TXD C) T0 D) T1

13. If the signal EA (active low) of 8051 ….. is not accessed [ ]

A) Internal program B) external program

C) Internal data D) external data

14. If the timer registers are incremented by the internal clock pulses from microcontrollers, the operation is called… [ ]

A) Counting B) timing C) both D) none

15. SFR address of TMOD is [ ]

A) 8CH B) 8AH C) 89H D) 8BH

16. Timer mode 0 is a….timer [ ]

A) 12-bit B) 11-bit C) 13-bit D) 15-bit

17. Mode 3 of timer in 8051 is…timer mode [ ]

A) 13-bit B) 16-bit C) split D) Timer auto reload

18. 8051 has… interrupts [ ]

A) 2 B) 3 C) 4 D) 5

19. Interrupt priorities of 8051 can be controlled by… [ ]

A) TCON B) PCON C) IP D) SP

20. D0 bit of IE register in 8051 is: [ ]

A) ES B) EA C) ET1 D) EX0

21. 21.D1 bit of TCON register in 8051 is [ ]

A) IE0 B) IT1 C) TF1 D)TF0

22. The technique of having the same address for two different registers is called…. [ ]

A) Single Buffering B) double buffering C) both D) none

23. Transmission in 8051 is initiated by writing a data to the …..SFR register [ ]

A) TCON B) PCON C) SBUF D) IP

24. MSB bit of… register is used to double the baud rate of serial transmission and reception [ ]

A) TCON B) PCON C) SBUF D) IP

25. ... and ….Bits of SCON register define the operating modes of the serial port [ ]

A) D1 and D2 B) D7 and D6

C) D4 and D5 D) D2 and D3

26. ….. in 8051 is used as multiprocessor communication enable bit [ ]

A) SM0 B) SM1 C) SM2 D) T1

27. In mode 2 of 8051, …bits are transmitted through TXD or received through RXD [ ]

A) 9 B) 10 C) 11 D) 12

28. 28. The baud rate in mode 0 is fixed at the shift clock frequency of….. [ ]

A) System clock freq/8 B) system clock freq/12

C) System clock freq/32 D) system clock freq/64

29. Find out the incorrect statements about 8051 serial ports [ ]

A) Half duplex operation B) Receive-buffered

C) Four different modes of operation

D) Option to use fixed or programmable baud rate

30. The processor 8051 can be revoked from the idle mode by applying a ….signal [ ]

A) Software interrupts B) hardware interrupt

C) Hardware reset D) both b and c

31. Internal data memory of 8051 is… [ ]

A) 128KB B) 64KB C) 4KB D) 32KB

32. 19th pin of IC 8051 is [ ]

A) RST B) ALE C) XTAL1 D) XTAL2

33. . ….. is an assembler directive that puts a byte constant at the memory location specified [ ]

A) ORG B) DB C) DW D) DBIT

34. In 8051, The Read strobe signal is given by.. [ ]

A) PSEN B) IE C) EA D) ALE

35. D4 bit of TCON is: [ ]

A) TF1 B) TF0 C) TR0 D) TR1

36. Split timer mode is applicable only for timer… [ ]

A) 0 B) 1 C) 2 D) 3

37. 8051 microcontrollers when operated as counters can count pulses applied on the External pin.....in timer 0 [ ]

A) P3.1 B) P3.2 C) P3.3 D) P3.4

38. ….has the highest interrupt priority in 8051 [ ]

A) External 0 B) External 1 C) Timer 1 D) Timer 0

39. 8-bit UART with variable baud rate is achieved by serial mode… [ ]

A) 0 B) 1 C) 2 D) 3

40. 9-bit UART with FOSC/64 is achieved by serial mode… [ ]

A) 0 B) 1 C) 2 D) 3

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